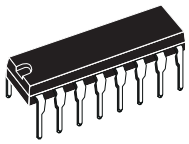
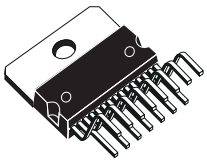
L6221AS L6221AD L6221N

QUAD DARLINGTON SWITCH

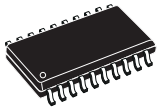
- FOUR NON INVERTING INPUTS WITH ENABLE
- OUTPUT VOLTAGE UP TO 50 V
- OUTPUT CURRENT UP TO 1.8 A
- VERY LOW SATURATION VOLTAGE
- TTL COMPATIBLE INPUTS
- INTEGRAL FAST RECIRCULATION DIODES



Powerdip 12 + 2 + 2



Multiwatt 15



SO16+2+2

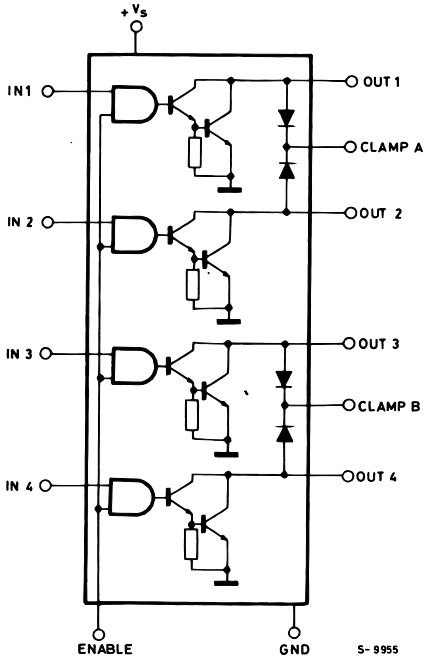
ORDERING NUMBERS:
L6221AS (Powerdip)
L6221N (Multiwatt15)
L6221AD (SO16+2+2)

DESCRIPTION

The L6221 monolithic quad darlington switch is designed for high current, high voltage switching applications. Each of the four switches is controlled by a logic input and all four are controlled by a common enable input. All inputs are TTL-compatible for direct connection to logic circuits.

Each switch consists of an open-collector darlington transistor plus a fast diode for switching applications with inductive device loads. The emitters of the four switches are commoned. Any number of inputs and outputs of the same device may be paralleled.

BLOCK DIAGRAM

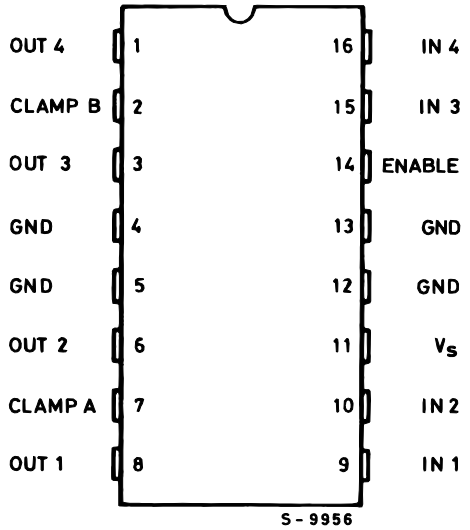


THERMAL DATA

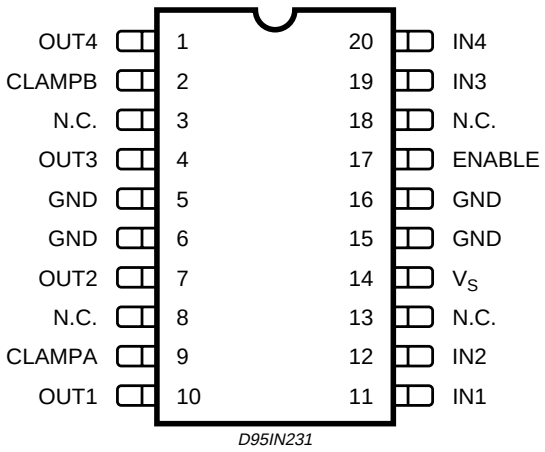
Symbol	Parameter		SO20	Powerdip	Multiwatt15	Unit
$R_{th\ j\text{-}pins}$	Thermal Resistance Junction-pins	Max.	17	14	–	°C/W
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Max.	–	–	3	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	Max.	80	80	35	°C/W

PIN CONNECTIONS (top views)

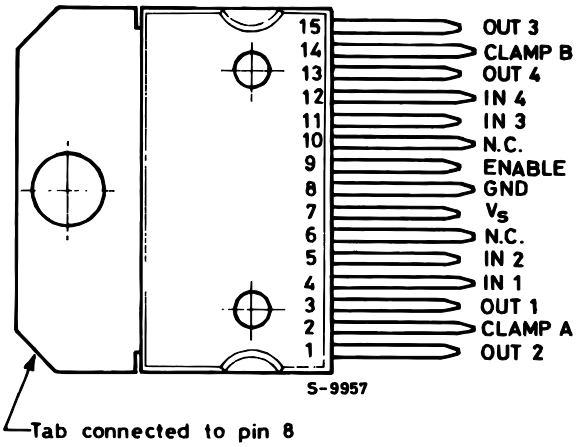
L6221AS (Powerdip)



L6221AD (SO16+2+2)



L6221N (Multiwatt-15)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_o	Output Voltage	50	V
V_s	Logic Supply Voltage	7	V
V_{IN}, V_{EN}	Input Voltage, Enable Voltage	V_s	
I_C	Continuous Collector Current (for each channel)	1.8	A
I_C	Collector Peak Current (repetitive, duty cycle = 10 % t_{on} = 5 ms)	2.5	A
I_C	Collector Peak Current (non repetitive, t = 10 µs)	3.2	A
T_{op}	Operating Temperature Range (junction)	– 40 to + 150	°C
T_{stg}	Storage Temperature Range	– 55 to + 150	°C
I_{sub}	Output Substrate Current	350	mA
P_{tot}	Total Power Dissipation at T_{pins} = 90 °C (powerdip) at T_{case} = 90 °C (multiwatt) at T_{case} = 90 °C (SO20) at T_{amb} = 70 °C (powerdip) at T_{amb} = 70 °C (multiwatt) at T_{amb} = 70 °C (SO20)	4.3 20 3.5 1 2.3 1	W W W W W W

TRUTH TABLE

Enable	Input	Power Out
H	H	ON
H	L	OFF
L	X	OFF

For each input : H = High level
L = Low level

PIN FUNCTIONS (see block diagram)

Name	Function
IN 1	Input to Driver 1
IN 2	Input to Driver 2
OUT 1	Output of Driver 1
OUT 2	Output of Driver 2
CLAMP A	Diode Clamp to Driver 1 and Driver 2
IN 3	Input to Driver 3
IN 4	Input to Driver 4
OUT 3	Output of Driver 3
OUT 4	Output of Driver 4
CLAMP B	Diode Clamp to Driver 3 and Driver 4
ENABLE	Enable Input to All Drivers
V_S	Logic Supply Voltage
GND	Common Ground

ELECTRICAL CHARACTERISTICS

Refer to the test circuit to Fig. 1 to Fig. 9 (V_S = 5V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min .	Typ .	Max .	Unit
V_S	Logic Supply Voltage		4.5		5.5	V
I_s	Logic Supply Current	All Outputs ON, I_C = 0.7A All Outputs OFF			20 20	mA mA
$V_{CE(sus)}$	Output Sustaining Voltage	V_{IN} = V_{IN}L, V_{EN} = V_{EN}H I_C = 100 mA	46			V
I_{CEX}	Output Leakage Current	V_{CE} = 50V V_{IN} = V_{IN}L, V_{EN} = V_{EN}H			1	mA
$V_{CE(sat)}$	Collector Emitter Saturation Voltage (one input on ; all others inputs off.)	V_s = 4.5V V_{IN} = V_{IN}H, V_{EN} = V_{EN}H I_C = 0.6A I_C = 1A I_C = 1.8A			 1 1.2 1.6	V
V_{IN}L, V_{EN}L	Input Low Voltage				0.8	V
I_{IN}L, I_{EN}L	Input Low Current	V_{IN} = V_{IN}L, V_{EN} = V_{EN}L			– 100	µ A
V_{IN}L, V_{EN}H	Input High Voltage		2.0			V
I_{IN}H , I_{EN}H	Input High Current	V_{IN} = V_{IN}H, V_{EN} = V_{EN}H			± 10	µ A
I_R	Clamp Diode Leakage Current	V_R = 50 V, V_{EN} = V_{EN}H V_{IN} = V_{IN}L			100	µ A
V_F	Clamp Diode Forward Voltage	I_F = 1A I_F = 1.8A			1.6 2.0	V V
$t_{d\ (on)}$	Turn on Delay Time	V_p = 5V, R_L = 10Ω			2	µ s
$t_{d\ (off)}$	Turn off Delay Time	V_p = 5V, R_L = 10Ω			5	µ s
ΔI_s	Logic Supply Current Variation	V_{IN} = 5V, V_{EN} = 5V I_{out} = – 300 mA for Each Channel			120	m A