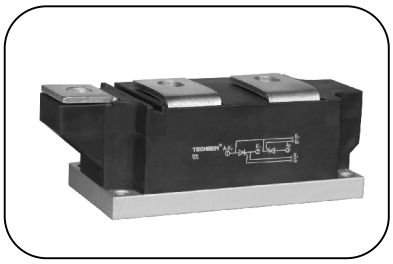
TECHSEM

MTC500 MTA500 MTK500 MTX500 MT500
Thyristor Modules



Features：

- Isolated mounting base 3000V~
- Pressure contact technology with Increased power cycling capability
- Space and weight saving

Typical Applications

- AC/DC Motor drives
- Various rectifiers
- DC supply for PWM inverter

V_{DSM},V_{RSM}	V_{DRM},V_{RRM}	Type & Outline
900V	800V	MTx500-08-416F3
1100V	1000V	MTx500-10-416F3
1300V	1200V	MTx500-12-416F3
1500V	1400V	MTx500-14-416F3
1700V	1600V	MTx500-16-416F3
1900V	1800V	MTx500-18-416F3

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	T_j(°C)	VALUE			UNIT
				Min	Type	Max	
$I_{T(AV)}$	Mean on-state current	180° half sine wave 50Hz Single side cooled,T_c=85°C	125			500	A
$I_{T(RMS)}$	RMS on-state current		125			785	A
I_{DRM} I_{RRM}	Repetitive peak current	at V_{DRM} at V_{RRM}	125			35	mA
I_{TSM}	Surge on-state current	10ms half sine wave V_R=60%V_{RRM}	125			14.5	KA
I^2t	I^2T for fusing coordination					1051	A^2s*10^3
V_{TO}	Threshold voltage		125			0.80	V
r_T	On-state slop resistance					0.34	mΩ
V_{TM}	Peak on-state voltage	I_{TM}=1600A	25			1.54	V
dv/dt	Critical rate of rise of off-state voltage	V_{DM}=67%V_{DRM}	125			1000	V/μs
di/dt	Critical rate of rise of on-state current	Gate source 1.5A t_r≤0.5μs Repetitive	125			200	A/μs
I_{GT}	Gate trigger current	V_A=12V, I_A=1A	25	30		200	mA
V_{GT}	Gate trigger voltage			1.0		3.0	V
I_H	Holding current			20		200	mA
V_{GD}	Non-trigger gate voltage	V_{DM}=67%V_{DRM}	125	0.2			V
$R_{th(j-c)}$	Thermal resistance Junction to case	Single side cooled per chip				0.065	°C /W
$R_{th(c-h)}$	Thermal resistance case to heatsink	Single side cooled per chip				0.024	°C /W
V_{iso}	Isolation voltage	50Hz,R.M.S,t=1min,I_{iso}:1mA(MAX)		3000			V
F_m	Thermal connection torque(M10)				12.0		N·m
	Mounting torque(M6)				6.0		N·m
T_{stg}	Stored temperature			-40		125	°C
W_t	Weight				1430		g
Outline	416F3						

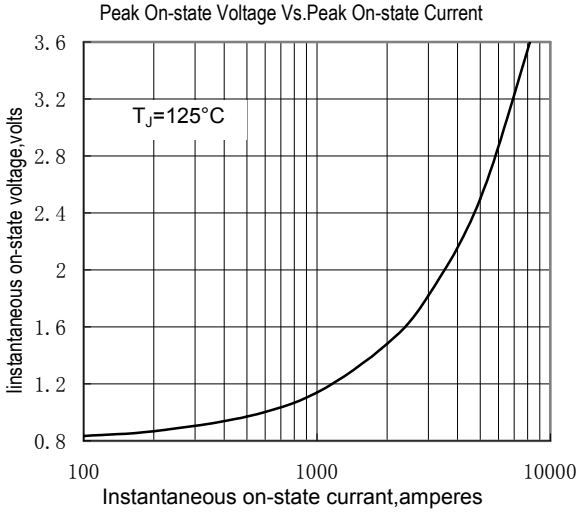


Fig.1

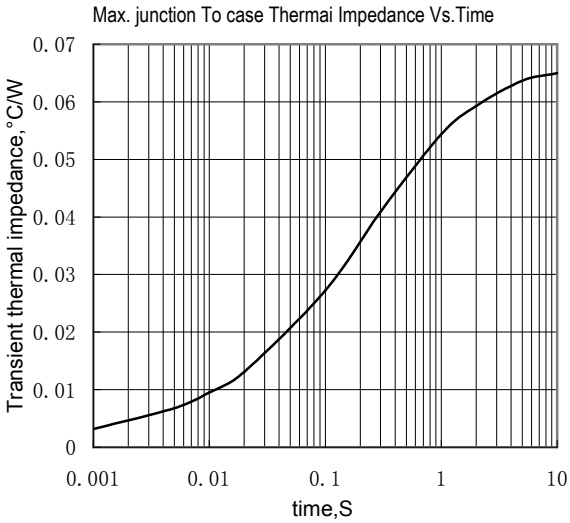


Fig.2

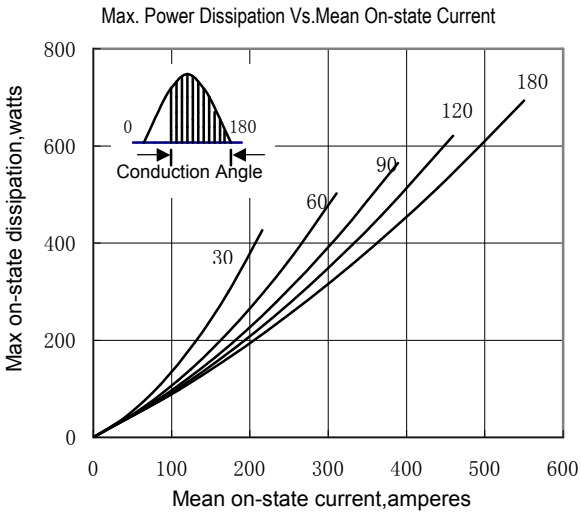


Fig.3

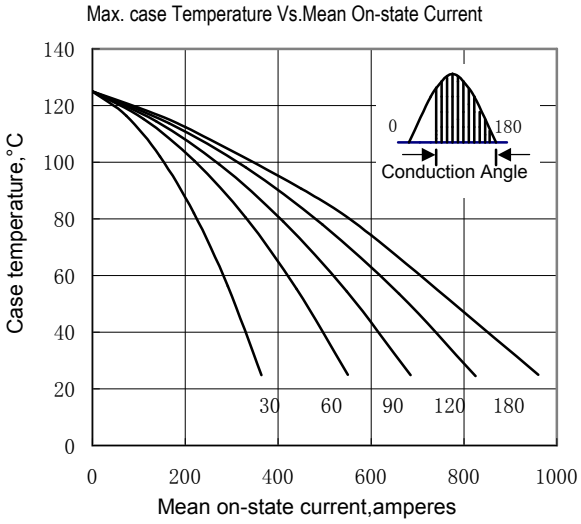


Fig.4

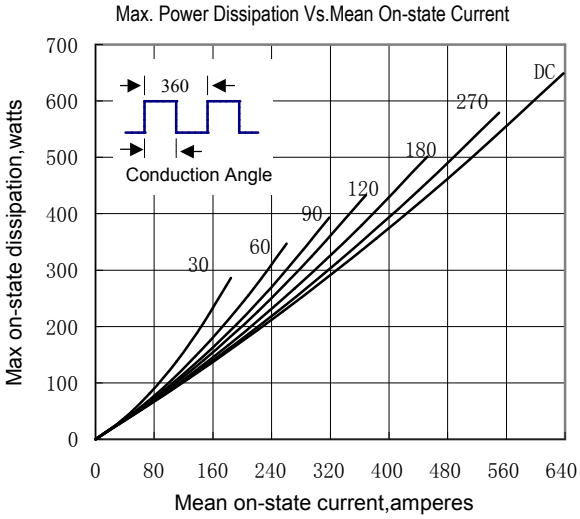


Fig.5

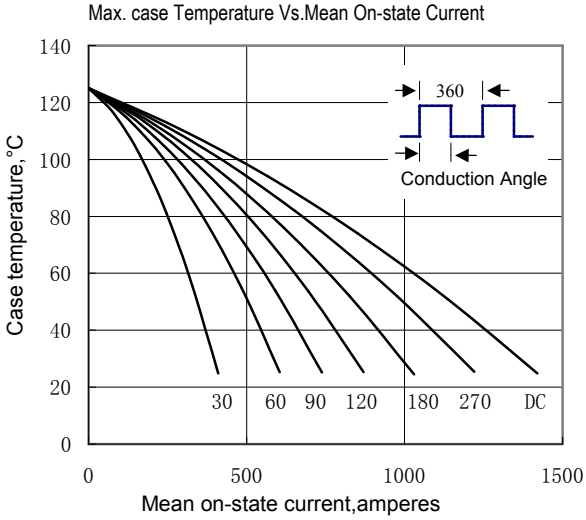


Fig.6

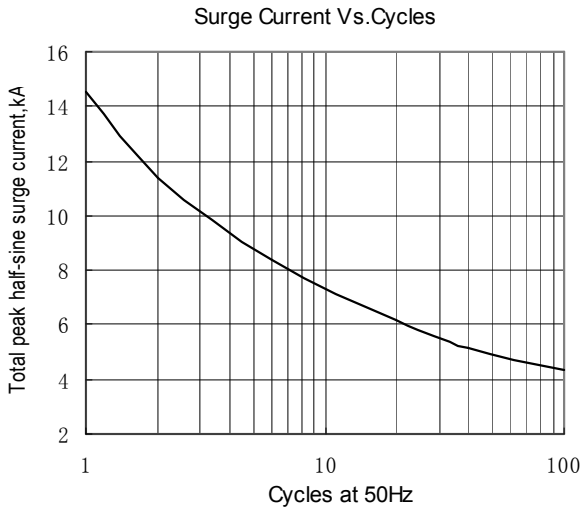


Fig.7

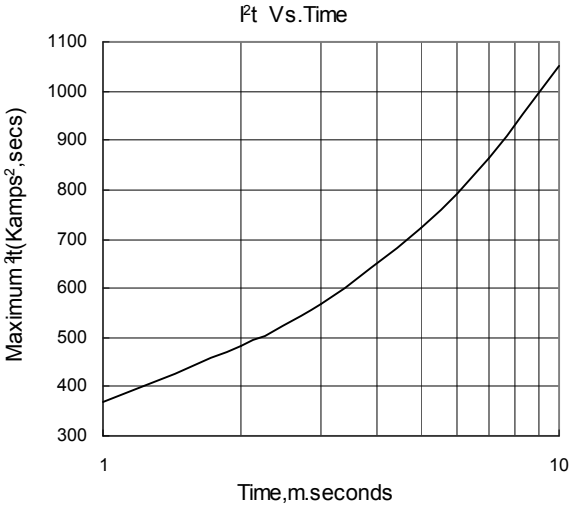


Fig.8

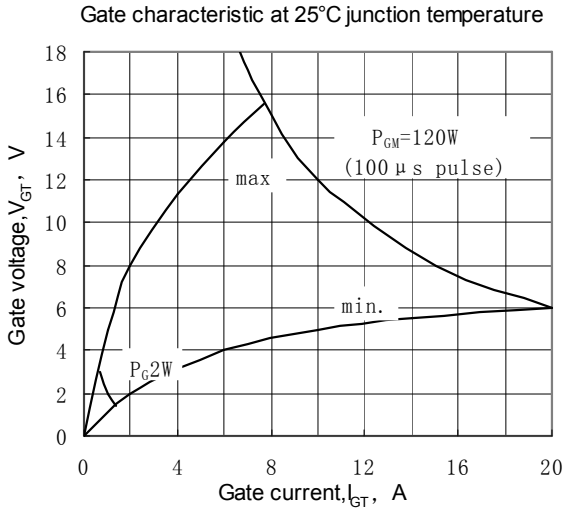


Fig.9

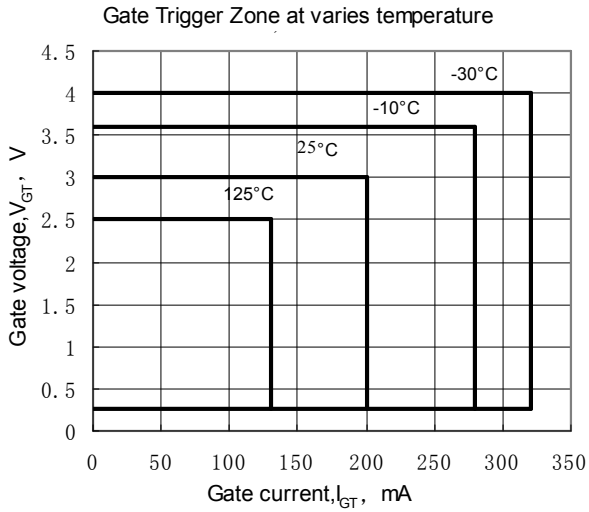


Fig.10

Outline: