



Advanced  
Micro  
Devices

# PALCE610 Family

EE CMOS High Performance Programmable Array Logic

## DISTINCTIVE CHARACTERISTICS

- AMD's Programmable Array Logic (PAL) architecture
- Electrically-erasable CMOS technology providing half power (90 mA I<sub>CC</sub>) at high speed
  - 15 = 15 ns t<sub>PD</sub>
  - 25 = 25 ns t<sub>PD</sub>
- Sixteen macrocells with configurable I/O architecture
- Registered or combinatorial operation
- Registers programmable as D, T, J-K, or S-R
- Asynchronous clocking via product term or bank register clocking from external pins
- Register preload for testability
- Power-up reset for initialization
- Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages
- Fully tested for 100% programming yield and high reliability
- Extensive third-party software and programmer support through FusionPLD partners

## GENERAL DESCRIPTION

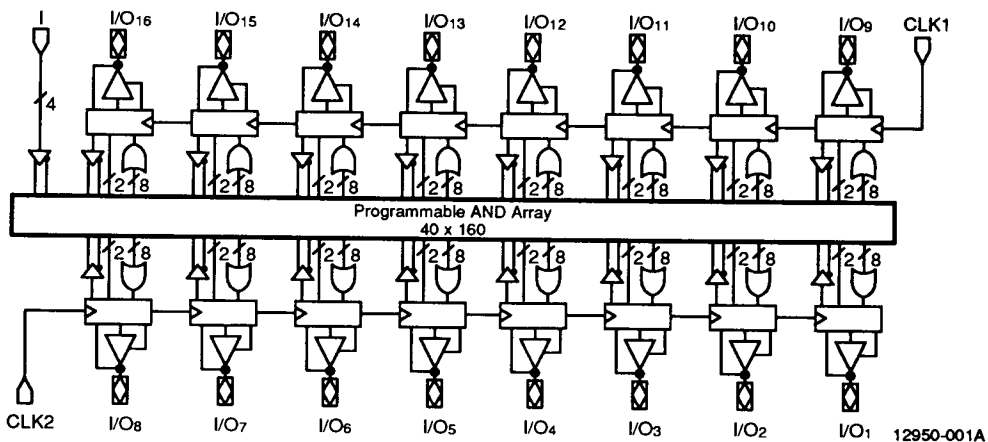
The PALCE610 is a general purpose PAL device and is functionally and fuse map equivalent to the EP610. It can accommodate logic functions with up to 20 inputs and 16 outputs. There are 16 I/O macrocells that can be individually configured to the user's specifications. The macrocells can be configured as either registered or combinatorial. The registers can be configured as D, T, J-K, or S-R flip-flops.

The PALCE610 uses the familiar sum-of-products logic with programmable-AND and fixed-OR structure. Eight product terms are brought to each macrocell to provide logic implementations.

The PALCE610 is manufactured using advanced CMOS EE technology providing high density and low power consumption. Moreover, it is a high-speed device having a worst-case t<sub>PD</sub> of 15 ns. Space-saving 24-pin SKINNYDIP and 28-pin PLCC packages are offered.

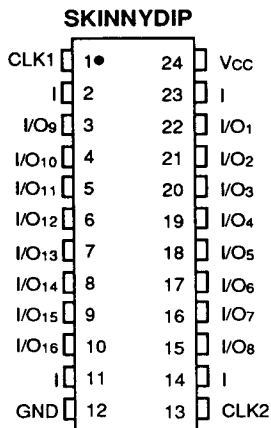
This device can be quickly erased and reprogrammed providing for easy prototyping. Once a device is programmed the security bit can be used to provide protection from copying a proprietary design.

## BLOCK DIAGRAM

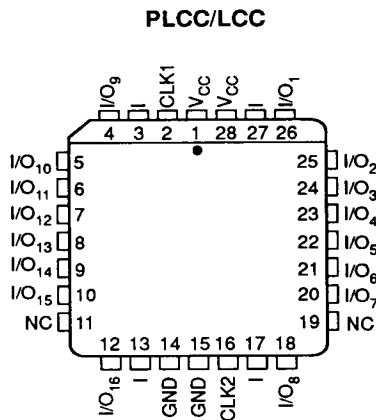


**CONNECTION DIAGRAMS**

**Top View**



12950-002A



12950-003A

**Note:**  
Pin 1 is marked for orientation

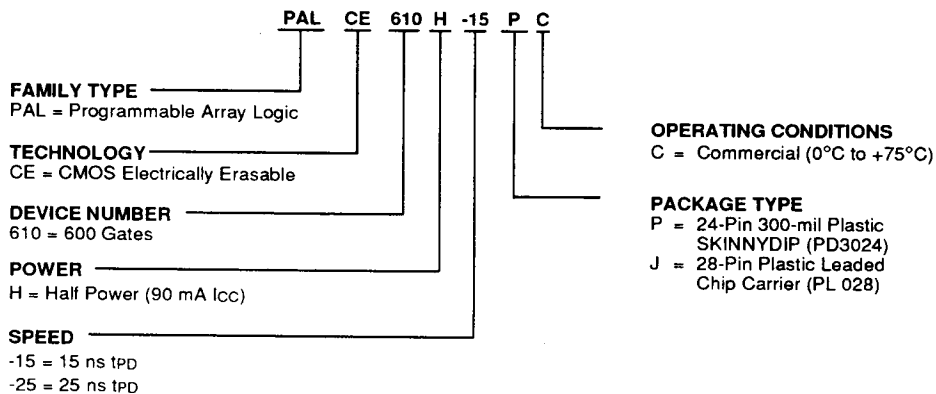
**PIN DESIGNATIONS**

- CLK      Clock
- GND      Ground
- I          Input
- I/O       Input/Output
- NC        No Connect
- Vcc       Supply Voltage

## ORDERING INFORMATION

### Commercial Products

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-15	PC, JC
PALCE610H-25	

#### Valid Combinations

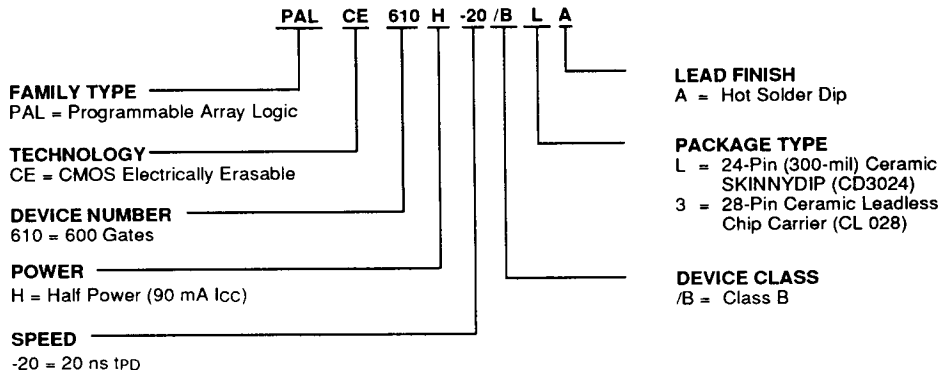
The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

**ORDERING INFORMATION**

**APL Products**

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
PALCE610H-20	/BLA,/B3A

**Valid Combinations**

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

**Group A Tests**

Group A tests consist of Subgroups 1, 2, 3, 7, 8, 9, 10, 11.

**Military Burn-in**

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.

## FUNCTIONAL DESCRIPTION

The PALCE610 is a general purpose programmable logic device. It has 16 independently-configurable macrocells. Each macrocell can be configured as either combinatorial or registered. The registers can be D, T, J-K, or S-R type flip-flops. The device has 4 dedicated input pins and 2 clock pins. Each clock pin controls 8 of the 16 macrocells.

The programming matrix implements a programmable AND logic array which drives a fixed OR logic array. Buffers for device inputs have complementary outputs to provide user-programmable input polarity. Unused input pins should be tied to  $V_{cc}$  or ground.

The array uses AMD's electrically erasable technology. An unprogrammed bit is disconnected and a programmed bit is connected. Product terms with all bits unprogrammed assume the logical-HIGH state and product terms with both the TRUE and Complement bits programmed assume the logical-LOW state.

The programmable functions in the PALCE610 are automatically configured from the user's design specifications, which can be in a number of formats. The design specification is processed by development software to verify the design and create a programming file. This file, once downloaded to the programmer, configures the design according to the user's desired function.

### Macrocell Configurations

The PALCE610 macrocell can be configured as either combinatorial or registered. Both the combinatorial and registered configurations have output polarity control. The register can be configured as a D, T, J-K, or S-R type flip-flop. Figure 1 shows the possible configurations.

Each macrocell can select as its clock either the corresponding clock pin or the CLK/OE product term. If the clock pin is selected, the output enable is controlled by the CLK/OE product term. If the CLK/OE product term is selected, the output is always enabled.

### Combinatorial I/O

All 8 product terms are available to the OR gate. The output-enable function is performed by the CLK/OE product term.

### Registered Configurations

There are 4 flip-flop types available: D, T, J-K and S-R.

The registers can be configured as synchronous or asynchronous. In the synchronous configuration, the clock is controlled by the clock input pin. The output enable is controlled by the product term function. In the asynchronous configuration, the clock input is controlled by the product term. The output is always enabled.

In The D and T configurations, feedback can be either from Q or the output pin. This allows D and T configurations to be either outputs or I/O. In the J-K and S-R configurations, feedback is only from Q; therefore, J-K and S-R configurations are strictly outputs.

### D Flip-Flop

All 8 product terms are available to the OR gate. The D input polarity is controlled by an exclusive-OR gate. For the D flip-flop, the output level is the D-input level at the rising edge of the clock.

D	$Q^n$	$Q^{n+1}$
0	0	0
0	1	0
1	0	1
1	1	1

### T Flip-Flop

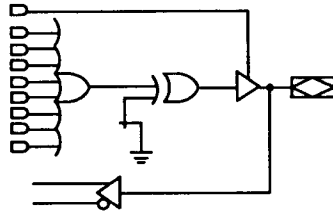
All 8 product terms are available to the OR gate. The T input polarity is controlled by an exclusive-OR gate. For the T register, the output level toggles when the T input is HIGH and remains the same when the T input is LOW.

T	$Q^n$	$Q^{n+1}$
0	0	0
0	1	1
1	0	1
1	1	0

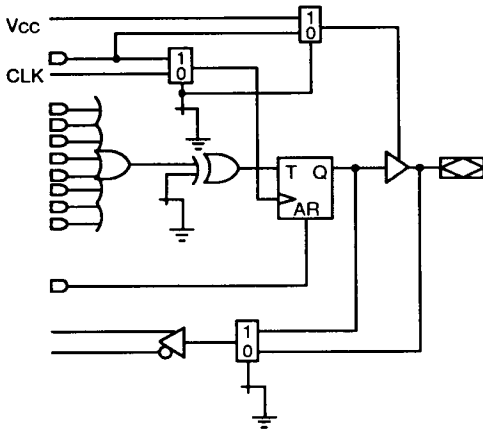
### J-K Flip-Flop

The 8 product terms are divided between the J and K inputs. N product terms go to the J input and 8-N product terms go to the K input, where N can range from 0 to 8. Both the J and K inputs to the flip-flop have polarity control via exclusive-OR gates. The J-K flip-flop operation is shown below.

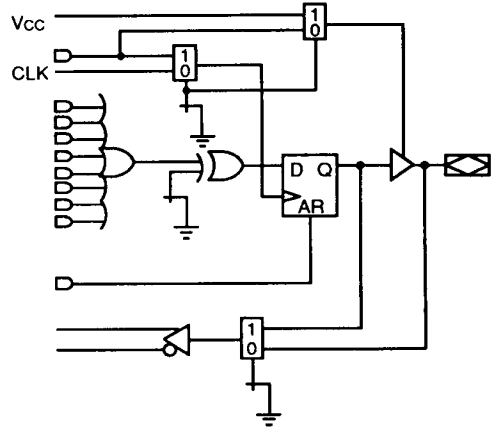
J	K	$Q^n$	$Q^{n+1}$
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0



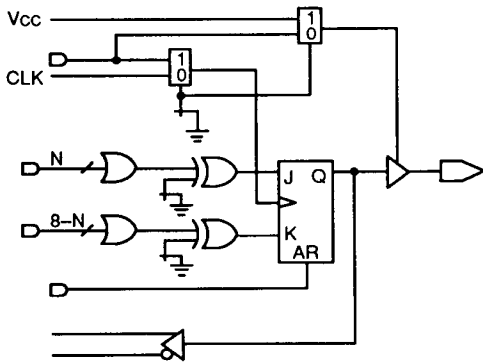
Combinatorial



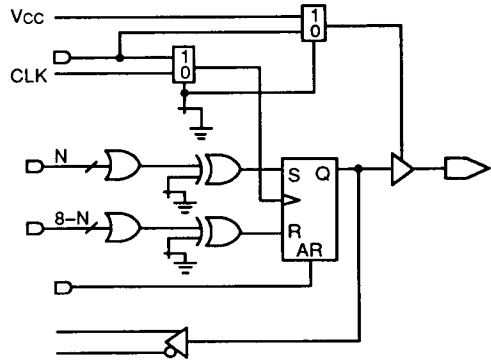
T Register



D Register



J-K Register



S-R Register

Figure 1. Macrocell Configurations

12950-004A

## S-R Flip-Flop

The 8 product terms are divided between the S and R inputs. N product terms go to the S input and 8-N product terms go to the R input, where N can range from 0 to 8. Both the S and R inputs to the flip-flop have polarity control via exclusive-OR gates. The S-R flip-flop operation is shown below.

S	R	Q <sup>n</sup>	Q <sup>n+1</sup>
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	Not Allowed	

## Asynchronous Reset

All flip-flops have an asynchronous-reset product-term input. When the product term is true, the flip-flop will reset to a logic LOW, regardless of the clock and data inputs.

## Power-Up Reset

All flip-flops power up to a logic LOW for predictable system initialization. Outputs of the PALCE610 depend on whether they are selected as registered or combinatorial. If registered is selected, the output will be LOW. If combinatorial is selected, the output will be a function of the logic. The V<sub>cc</sub> rise must be monotonic and the reset delay time is 1000 ns maximum.

## Register Preload

The register on the PALCE610 can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle

through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

## Security Bit

After programming and verification, a PALCE610 design can be secured by programming the security bit. Once programmed, this bit defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. However, programming and verification are also defeated by the security bit. The bit can only be erased in conjunction with the array during the erase cycle. Preload is not affected by the security bit.

## Technology

The PALCE610 is manufactured using AMD's advanced Electrically Erasable (EE) CMOS process. This technology uses an EE cell to replace the fuse link in bipolar parts, and allows AMD to offer lower-power parts of high complexity. In addition, since the EE cells can be erased and reprogrammed, these devices can be 100% factory tested before being shipped to the customer. Inputs and outputs are designed to be compatible with TTL devices. This technology provides strong input clamp diodes, output slew-rate control, and a grounded substrate for clear switching.

## Programming and Erasing

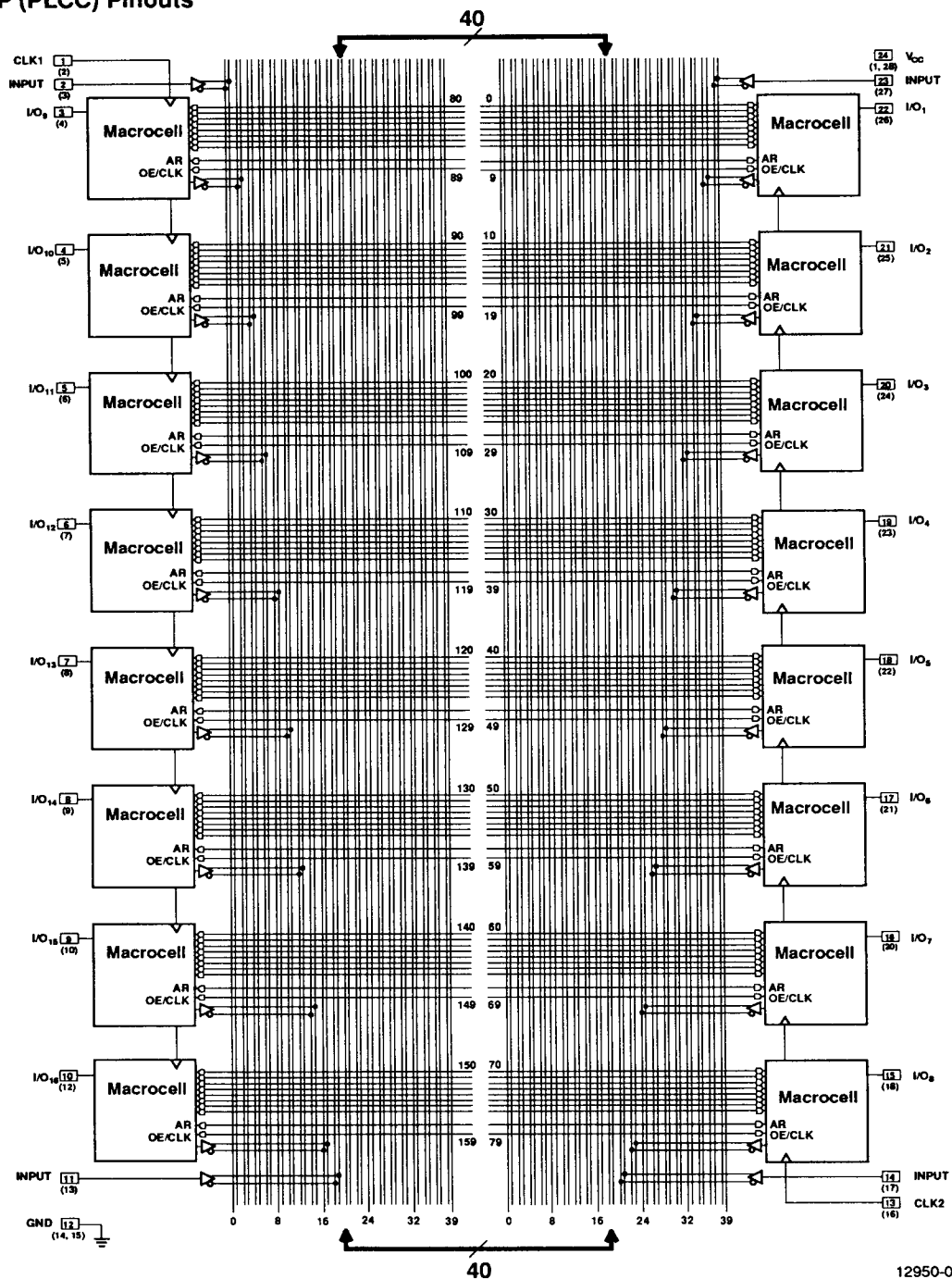
The PALCE610 can be programmed on standard logic programmers. It also may be erased to reset a previously configured device back to its virgin state. Bulk erase is automatically performed by the programming hardware. No special erase operation is required.

## CMOS Compatibility

The PALCE610 has CMOS-compatible outputs. The output voltage (V<sub>OH</sub>) is 3.85 V at -2.0 mA.

# PALCE610 LOGIC DIAGRAM

## DIP (PLCC) Pinouts



12950-005A



### ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_A = 0^\circ\text{C}$ to $+75^\circ\text{C}$ )	100 mA

### OPERATING RANGES

#### Commercial (C) Devices

Ambient Temperature ( $T_A$ )	Operating in Free Air	0°C to +75°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground		+4.75 V to +5.25 V

*Operating ranges define those limits between which the functionality of the device is guaranteed.*

*Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.*

### DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified (Note 2)

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit	
$V_{OH}$	Output HIGH Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	$I_{OH} = -4.0$ mA	2.4		V
			$I_{OH} = -2.0$ mA	3.84		V
$V_{OL}$	Output LOW Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	$I_{OL} = 8.0$ mA		0.5	V
			$I_{OL} = 4.0$ mA		0.45	V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V	
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V	
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.25$ V, $V_{CC} = \text{Max.}$ (Note 2)		10	$\mu\text{A}$	
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 2)		-10	$\mu\text{A}$	
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.25$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		10	$\mu\text{A}$	
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 2)		-10	$\mu\text{A}$	
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = \text{Max.}$ (Note 3)	-30	-150	mA	
$I_{CC}$	Supply Current	$V_{IN} = 0$ V, Outputs Open ( $I_{OUT} = 0$ mA) $V_{CC} = \text{Max.}$		90	mA	

#### Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and tester noise are included.
2. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation.

## CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 2.0 V	V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	Output Capacitance	V <sub>OUT</sub> = 2.0 V	T <sub>A</sub> = +25°C f = 1 MHz	8	

### Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

## SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 2)

Parameter Symbol	Parameter Description		-15		-25		Unit
			Min.	Max.	Min.	Max.	
t <sub>PD</sub>	Input or Feedback to Combinatorial Output			15	25		ns
t <sub>S</sub>	Setup Time from Input or Feedback to Clock		12		15		ns
t <sub>H</sub>	Hold Time		0		0		ns
t <sub>CO</sub>	Clock to Output			8	12		ns
t <sub>WL</sub>	Clock Width	LOW	6		10		ns
t <sub>WH</sub>		HIGH	6		10		ns
f <sub>MAX</sub>	Maximum Frequency (Note 3)	External Feedback	1/(t <sub>S</sub> + t <sub>CO</sub> )		50	37	MHz
		Internal Feedback (f <sub>CNT</sub> )		76.1	40	MHz	
		No Feedback		1/(t <sub>WH</sub> + t <sub>WL</sub> )		83.3	50
t <sub>EA</sub>	Input to Output Enable Using Product Term Control			15	25		ns
t <sub>ER</sub>	Input to Output Disable Using Product Term Control			15	25		ns
t <sub>AR</sub>	Asynchronous Reset to Registered Output			15	25		ns
t <sub>ARW</sub>	Asynchronous Reset Width		10		15		ns
t <sub>ARR</sub>	Asynchronous Reset Recovery Time			15	25		ns
t <sub>SA</sub>	Setup Time from Input or Feedback to Clock (Note 4)		5		8		ns
t <sub>HA</sub>	Hold Time (Note 4)		5		12		ns
t <sub>COA</sub>	Clock to Output (Note 4)			15	27		ns
t <sub>WLA</sub>	Clock Width	LOW (Note 4)	6		10		ns
t <sub>WHA</sub>		HIGH (Note 4)	6		10		ns
f <sub>MAXA</sub>	Maximum Frequency (Notes 3 and 4)	External Feedback	1/(t <sub>SA</sub> + t <sub>COA</sub> )		50	28.6	MHz
		Internal Feedback (f <sub>CNT</sub> )		61.6	29.4	MHz	
		No Feedback		1/(t <sub>WLA</sub> + t <sub>WHA</sub> )		83.3	50

### Notes:

- See Switching Test Circuit for test conditions.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
- These parameters are measured using the asynchronous product-term clock.

### ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-0.5 V to $V_{CC} + 0.5$ V
DC Output or I/O Pin Voltage	-0.5 V to $V_{CC} + 0.5$ V
Static Discharge Voltage	2001 V
Latchup Current ( $T_c = -55^\circ\text{C}$ to $+125^\circ\text{C}$ )	100 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

### OPERATING RANGES

#### Military (M) Devices (Note 1)

Operating Case Temperature ( $T_c$ )	-55°C to +125°C
Supply Voltage ( $V_{CC}$ ) with Respect to Ground	+4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

#### Note:

1. Military products are 100% tested at  $T_c = +25^\circ\text{C}$ ,  $+125^\circ\text{C}$  and  $-55^\circ\text{C}$ , per MIL-STD-883.

### DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit	
$V_{OH}$	Output HIGH Voltage	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$	$I_{OH} = -2$ mA	2.4		V
			$I_{OH} = -1$ mA	3.84		
$V_{OL}$	Output LOW Voltage	$I_{OL} = 4$ mA $V_{IN} = V_{IH}$ or $V_{IL}$ $V_{CC} = \text{Min.}$		0.5		V
$V_{IH}$	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0			V
$V_{IL}$	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8		V
$I_{IH}$	Input HIGH Leakage Current	$V_{IN} = 5.5$ V, $V_{CC} = \text{Max.}$ (Note 4)		10		$\mu\text{A}$
$I_{IL}$	Input LOW Leakage Current	$V_{IN} = 0$ V, $V_{CC} = \text{Max.}$ (Note 4)		-10		$\mu\text{A}$
$I_{OZH}$	Off-State Output Leakage Current HIGH	$V_{OUT} = 5.5$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		10		$\mu\text{A}$
$I_{OZL}$	Off-State Output Leakage Current LOW	$V_{OUT} = 0$ V, $V_{CC} = \text{Max.}$ $V_{IN} = V_{IH}$ or $V_{IL}$ (Note 4)		-10		$\mu\text{A}$
$I_{SC}$	Output Short-Circuit Current	$V_{OUT} = 0.5$ V, $V_{CC} = 5.0$ V, $T_A = 25^\circ\text{C}$ (Note 5)	-30	-150		mA
$I_{CC}$	Supply Current	Outputs Open ( $I_{OUT} = 0$ A) $V_{CC} = \text{Max.}$		90		mA

#### Notes:

2. For APL products, Group A, Subgroups 1, 2 and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
3.  $V_{IL}$  and  $V_{IH}$  are input conditions of output tests and are not themselves directly tested.  $V_{IL}$  and  $V_{IH}$  are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I/O pin leakage is the worst case of  $I_{IL}$  and  $I_{OZL}$  (or  $I_{IH}$  and  $I_{OZH}$ ).
5. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.  $V_{OUT} = 0.5$  V has been chosen to avoid test problems caused by tester ground degradation. This parameter is not 100% tested, but is evaluated at initial characterization and at anytime the design is modified where  $I_{OS}$  may be affected.

## CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditions		Typ.	Unit
$C_{IN}$	Input Capacitance	$V_{IN} = 2.0\text{ V}$	$V_{CC}$	8	pF
$C_{OUT}$	Output Capacitance	$V_{OUT} = 2.0\text{ V}$	$T_A = +25^\circ\text{C}$ $f = 1\text{ MHz}$	8	

### Note:

- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

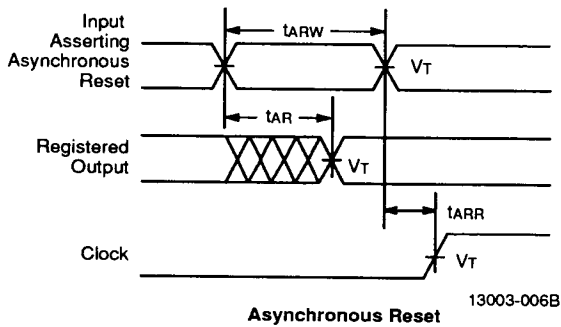
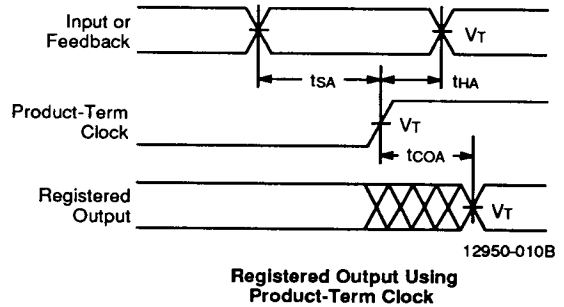
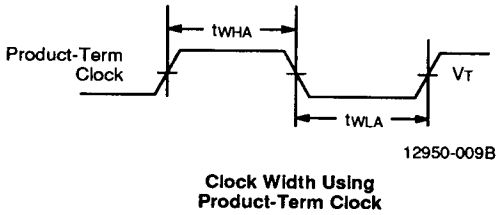
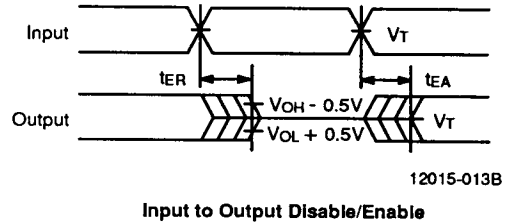
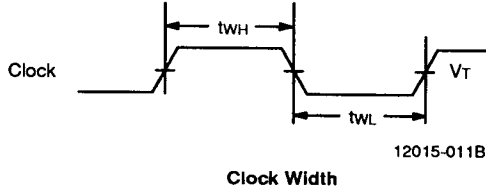
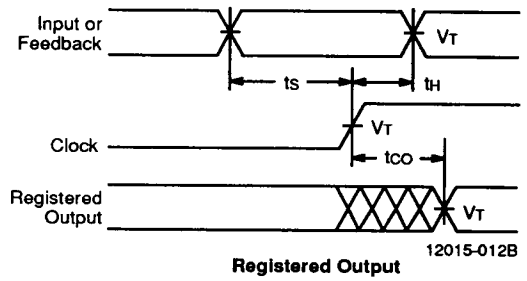
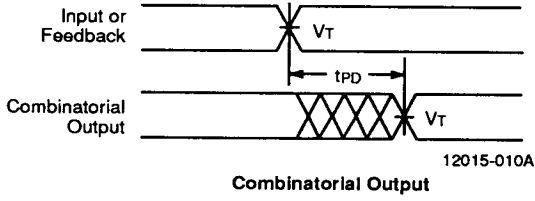
## SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Description		-20		Unit
			Min.	Max.	
$t_{PD}$	Input or Feedback to Combinatorial Output			20	ns
$t_s$	Setup Time from Input or Feedback to Clock		15		ns
$t_H$	Hold Time		0		ns
$t_{CO}$	Clock to Output			10	ns
$t_{WL}$	Clock Width	LOW	8		ns
$t_{WH}$		HIGH	8		ns
$f_{MAX}$	Maximum Frequency (Note 3)	External Feedback	$1/(t_s + t_{CO})$	40	MHz
		Internal Feedback ( $f_{CNT}$ )		50	MHz
		No Feedback	$1/(t_{WH} + t_{WL})$	62.5	MHz
$t_{EA}$	Input to Output Enable Using Product Term Control (Note 3)			20	ns
$t_{ER}$	Input to Output Disable Using Product Term Control (Note 3)			20	ns
$t_{AR}$	Asynchronous Reset to Registered Output			20	ns
$t_{ARW}$	Asynchronous Reset Width (Note 3)		20		ns
$t_{ARR}$	Asynchronous Reset Recovery Time (Note 3)			20	ns
$t_{SA}$	Setup Time from Input or Feedback to Clock (Note 4)		8		ns
$t_{HA}$	Hold Time (Note 4)		10		ns
$t_{COA}$	Clock to Output (Note 4)			20	ns
$t_{WLA}$	Clock Width	LOW (Note 4)	8		ns
$t_{WHA}$		HIGH (Note 4)	8		ns
$f_{MAXA}$	Maximum Frequency (Notes 3 and 4)	External Feedback	$1/(t_{SA} + t_{COA})$	35.8	MHz
		Internal Feedback ( $f_{CNT}$ )		45	MHz
		No Feedback	$1/(t_{WLA} + t_{WHA})$	52.6	MHz

### Notes:

- See Switching Test Circuit for test conditions. For APL Products, Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where frequency may be affected.
- These parameters are measured using the asynchronous product-term clock.

**SWITCHING WAVEFORMS**



**Notes:**

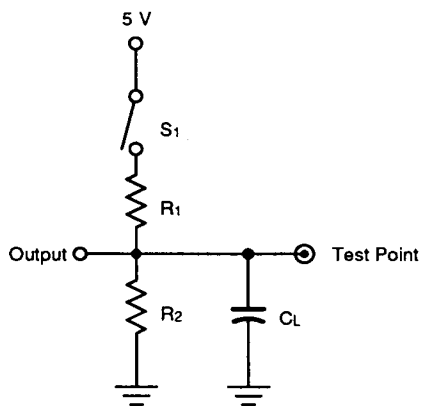
1.  $V_T = 1.5\text{ V}$
2. Input pulse amplitude 0 V to 3.0 V
3. Input rise and fall times 2–5 ns typical.

## KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Must be Steady	Will be Steady
	May Change from H to L	Will be Changing from H to L
	May Change from L to H	Will be Changing from L to H
	Don't Care; Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High-Impedance "Off" State

KS000010-PAL

## SWITCHING TEST CIRCUIT



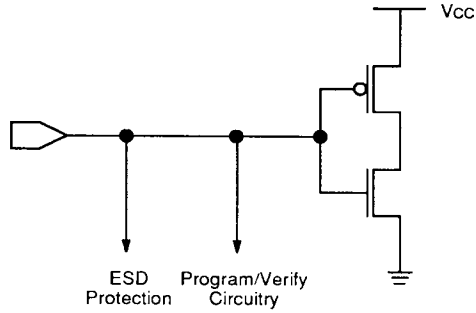
12950-012A

Specification	S <sub>1</sub>	C <sub>L</sub>	Commercial		Military		Measured Output Value
			R <sub>1</sub>	R <sub>2</sub>	R <sub>1</sub>	R <sub>2</sub>	
t <sub>PD</sub> , t <sub>CO</sub>	Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t <sub>EA</sub>	Z → H : Open Z → L : Closed	35 pF	855 Ω	340 Ω	855 Ω	340 Ω	1.5 V
t <sub>ER</sub>	H → Z : Open L → Z : Closed	5 pF	855 Ω	340 Ω	855 Ω	340 Ω	H → Z: V <sub>OH</sub> - 0.5 V L → Z: V <sub>OL</sub> + 0.5 V

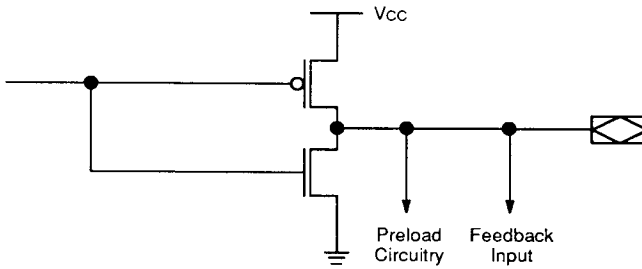
**ENDURANCE**

Symbol	Parameter Description	Test Conditions	Min.	Unit
t <sub>DR</sub>	Pattern Data Retention Time	Max. Storage Temperature	10	Years
		Max. Operating Temperature	20	Years
N	Reprogramming Cycles	Normal Programming Conditions	100	Cycles

**INPUT/OUTPUT EQUIVALENT SCHEMATICS**



**Typical Input**



**Typical Output**

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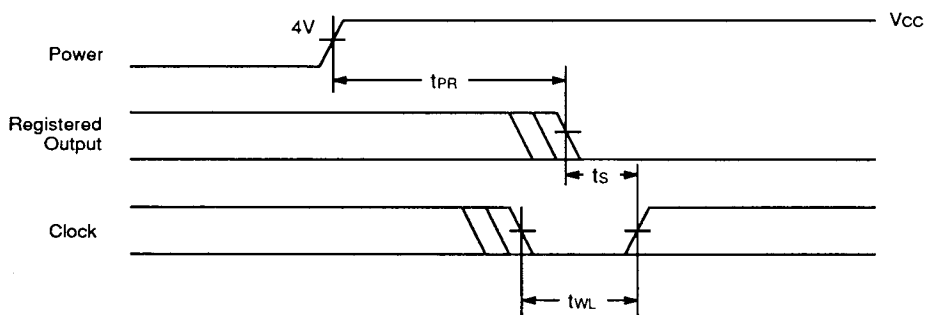
## Power-Up Reset

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up. This feature is valuable in simplifying state machine initialization. A timing diagram and parameter table are shown below. Due to the synchronous operation of the power-up reset and wide range of ways  $V_{CC}$  can rise to

its steady state, two conditions are required to insure a valid power-up reset. These conditions are:

1. The  $V_{CC}$  rise must be monotonic.
2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit
$t_{PR}$	Power-up Reset Time	1000	ns
$t_s$	Input or Feedback Setup Time	See Switching Characteristics	
$t_{wL}$	Clock Width LOW		



12950-007A

Power-Up Reset Waveform