UAA 145 · UAA 146

PHASE CONTROL CIRCUIT

T-65-09

Industrial Applications

Technology: Bipolar

Features:

- Separate pulse outputs for the positive and the negative half-cycle of the sync. signal
- Output pulse-width is freely adjustable
- Phase angle variable from >0° to <180°
- High-impedance phase shift input
- Less than 3° pulse symmetry between two half-cycles or phase of different integrated circuits
- Output pulse blocking

Case: DIP Special

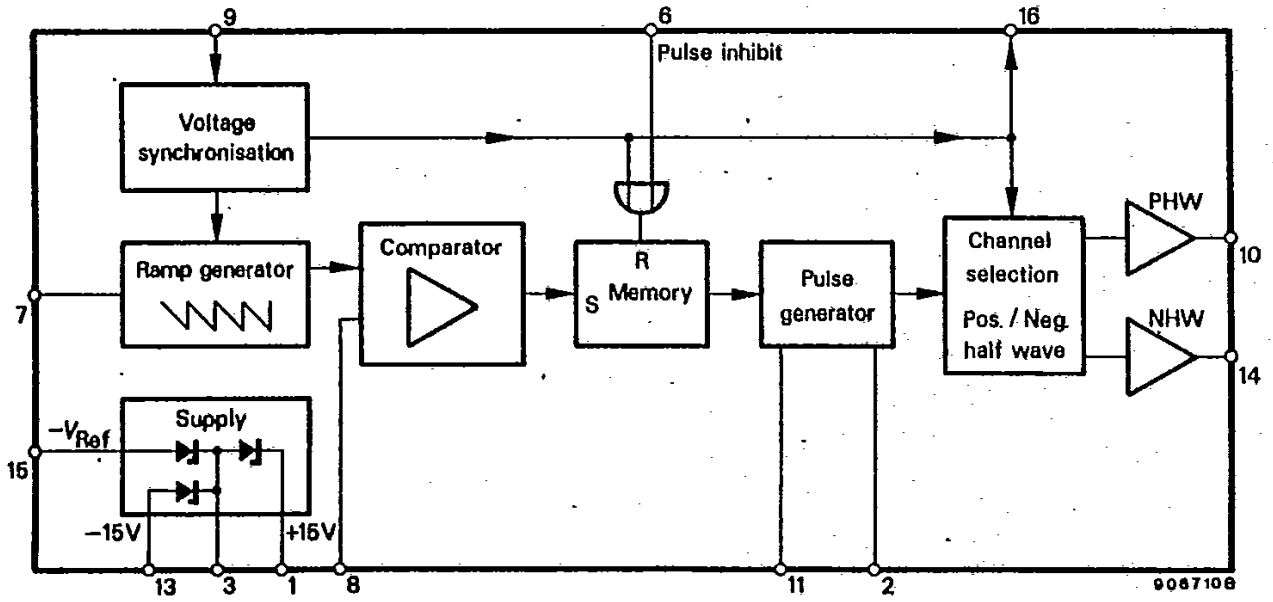

Fig. 1 Block diagram

Description

Phase control IC UAA 145 (or UAA 146) permits the number of components in thyristor drive circuits to be drastically reduced. The versatility of the device is further enhanced by the provision of a large number of pins giving access to internal circuit points. Beside the circuit description preliminary specifications as well as typical applications are given below.

The operation of the circuit is best explained with the aid of the block diagram shown in Fig. 1. It comprises a synchronizing stage, ramp generator, voltage comparator, pulse generator, channel selecting stage and two output amplifiers. The circuit diagrams are shown in Figs. 2 and 3. Also in Figs. 3 and 4 are shown the external components necessary for the operation and understanding of the circuit connected to the appropriate external terminals. As can be seen from Fig. 3, the circuit requires a +15 V and a −15 V supply rail. The positive voltage is applied directly to Pin 1, while an external series resistor in each line is used to connect the negative voltage Pin 13 and Pin 15. In the following circuit description each section of the block diagrams (Fig. 2 and 3) are discussed separately.

Sync. stage

Pin 9 is connected, via a voltage divider (22 kΩ and R_p), to the AC line (sync signal source). A pulse is generated during each zero crossover of the sync input. The pulse duration depends on the resistance R_p and has a value 50...100 µs. (Fig. 3).
In addition to providing zero voltage switching pulses this section of the circuit generates blocking signals for use in the channel selecting stage.

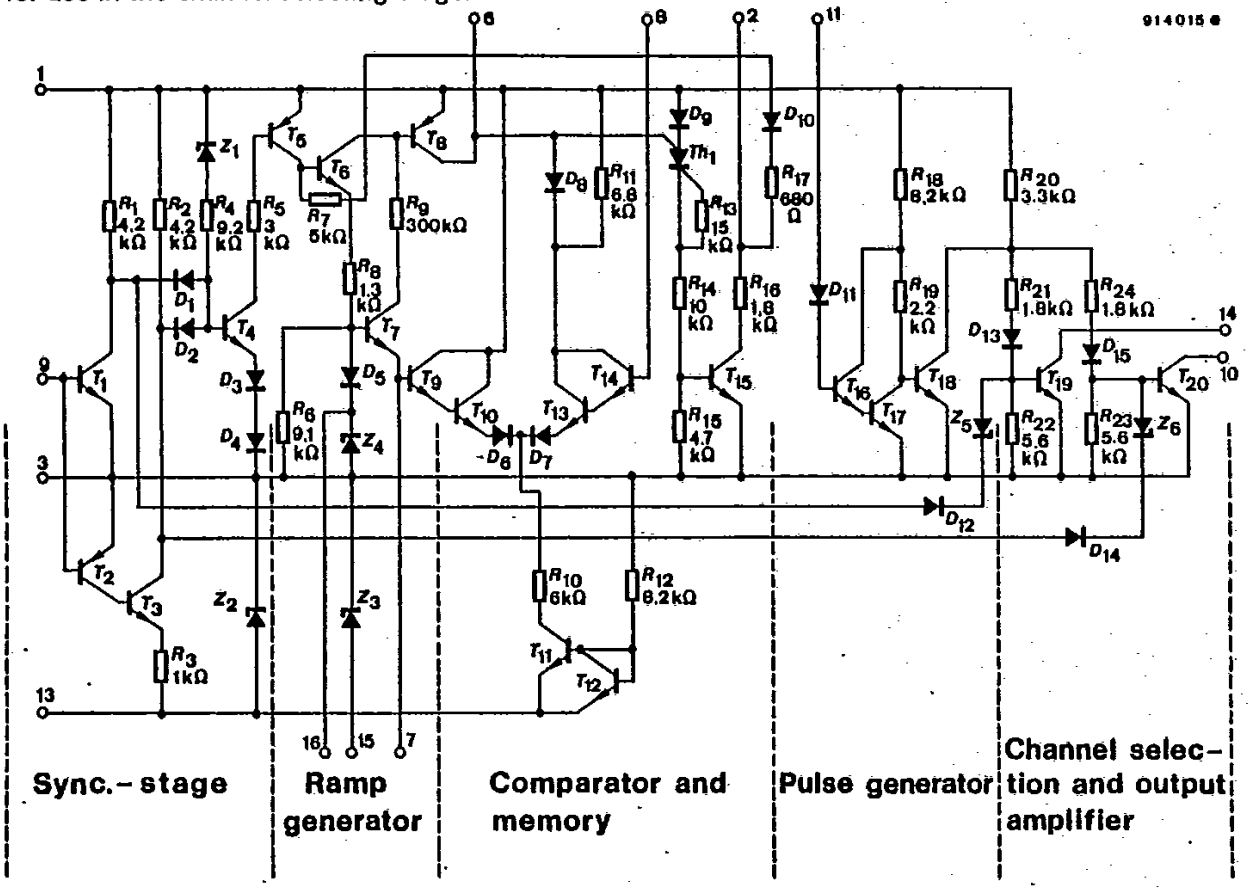

Fig. 2 IC diagram and pin connections

Ramp (Sawtooth) generator

Transistor T_7 amplifies the zero-crossover switching pulses. During the sync process capacitor C_s at Pin 7 is charged to the operating voltage of reference diode Z_4, i.e. to approximately 8.5 V, the charging time being always less than the duration of the sync pulse. The capacitor discharges via resistor R_s during each half-cycle. The discharge voltage is of the same magnitude as the charge voltage, and is determined by Z_3. To ensure an approximately linear ramp waveform, the voltage is allowed to decay up to ca. 0.7 C_sR_s. Because Z-diodes Z_3 and Z_4 have the same temperature characteristics, the timing of the ramp zero crossover point in relation to that of the sync pulse is constant, and consequently the pulse phasing rear limit is also very stable.

Comparator (Differential amplifier) and memory

In the voltage comparator stage the ramp voltage is compared with the shift voltage V_φ applied to Pin 8. The comparator switches whenever the instantaneous ramp voltage is the same as the shift voltage (corresponding to the desired phase angle), thereby causing the memory to be set, i.e. firing the thyristor Th_1 to be turned on . The time delay between the signal input and the comparator output signal is proportional to the required phase angle. Design of the circuit is such that the memory content is reset only during the instant of zero crossover, the reset signal always overriding the set signal. This effectively prevents the generation of additional output pulses and causes any pulse already started to be immediately inhibited on application of an inhibit signal to Pin 6. The memory content can also be reset via Pin 6. Thus the memory ensures that any noise (negative voltage transients) superimposed on the shift signal at Pin 8 cannot give rise to the generation of multiple pulses during the half-cycle.

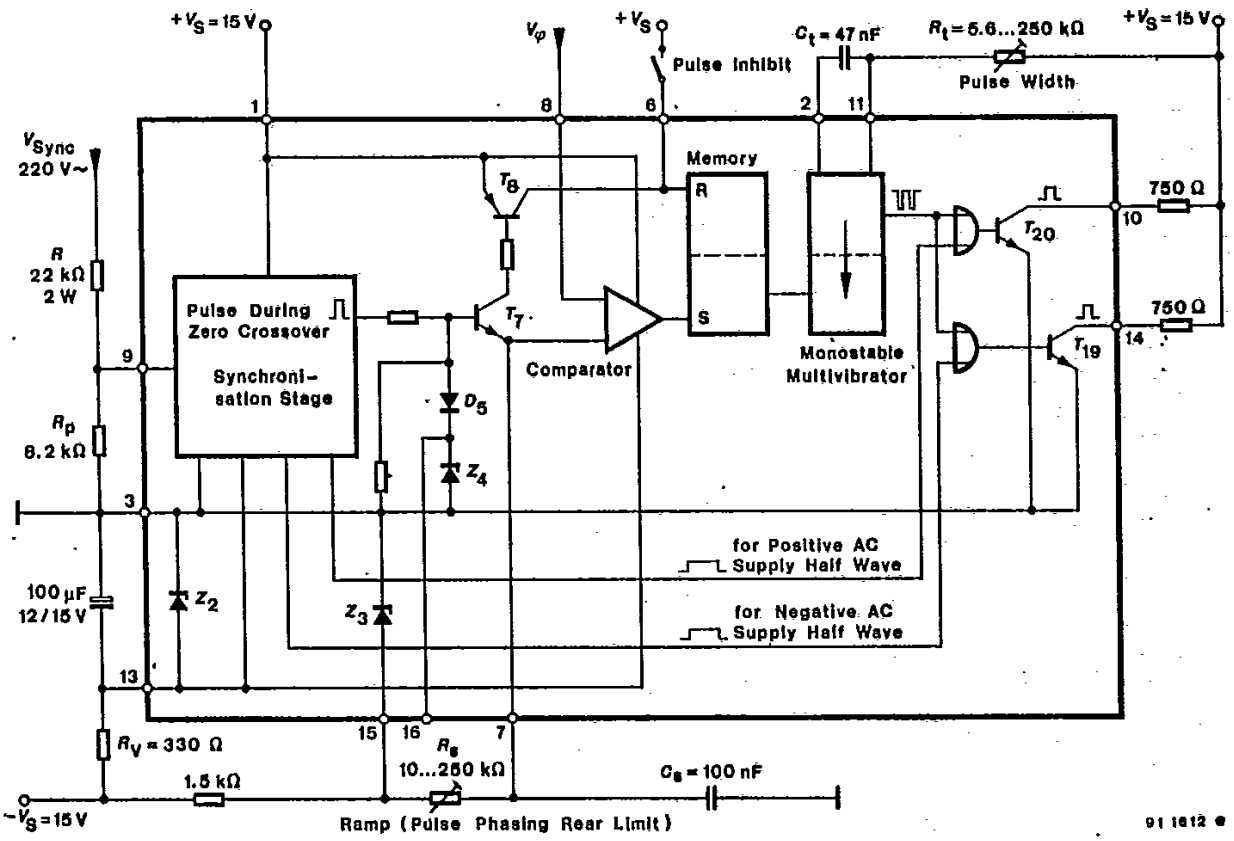

Fig. 3 Block diagram and basic circuit

Pulse generator

The memory setting pulse also triggers a monostable stage. The duration of the pulse produced by the monostable is determined by C_t and R_t, connected to Pin 2 and Pin 11.

Channel selection and output amplifier

A pulse is produced at either output Pin 10 or Pin 14 if transistor T_{20} or T_{19} respectively is cut off. The pulses derived from the pulse generator are applied to the output transistors via OR gates controlled by the half-cycle signals derived from the sync stage. During the positive half-cycle no signal is applied from the sync stage to T_{19} so that an output pulse is produced at Pin 14, the same is valid for Pin 10 during the negative half-cycle.

Absolute maximum ratings

Reference point Pin 3, $T_{amb} = 25$ °C, unless otherwise specified

Positive supply voltage	Pin 1	V_S	18	V
Shift voltage	Pin 8	V_φ	V_{S1}	V
		$-V_\varphi$	5	V
Reverse voltage, control input	Pin 11	$-V_{IR}$	15	V
Negative supply current	Pin 13	$-I_S$	25	mA
	Pin 15	$-I_S$	5	mA
Synchronisation current	Pin 9	$\pm I_{sync}$	20	mA
Control input pulse current	Pin 11	I_I	3	mA
Output currents	Pin 10	I_O	20	mA
	Pin 14	I_O	20	mA
Total power dissipation $T_{amb} \leqq 70$ °C		P_{tot}	550	mW
Junction temperature		T_j	125	°C
Ambient temperature range	**UAA 145**	T_{amb}	−25...+70	°C
	UAA 146	T_{amb}	0...70	°C
Storage temperature range		T_{stg}	−25...+125	°C

Max. thermal resistances

Junction ambient	R_{thJA}	100 K/W
Junction case	R_{thJC}	35 K/W

DC characteristics

$V_{S1} = 13...16$ V, $-V_{S13} = 15$ mA, reference point Pin 3, Fig 3, $T_{amb} = 25$ °C, unless otherwise specified

				Min.	Typ.	Max.	
Positive supply current							
$V_S = 16$ V	**UAA 145**	Pin 1	I_S	12		30	mA
	UAA 146	Pin 1	I_S	12		35	mA
Z-voltages Fig. 3							
$-I_{S13} = 15$ mA		Pin 13	$-V_Z$	7.0		9.0	V
$-I_{S15} = 3.5$ mA		Pin 15	$-V_Z$	7.0		9.0	V
$V_S = 13$ V, $V_{sync9} = 0$ V		Pin 16	V_Z	7.0		9.0	V
Shift current							
$V_S = 16$ V, $V_{\varphi 8} = 13$ V, $V_7 = 0$ V, $I_{Sync9} = 0.3$ mA		Pin 8	I_φ			10	µA
C_t–potential shift current							
$V_S = V_{I2} = 13$ V, $V_{I7} = 3$ V, $I_{\varphi 8} = 5$ µA, $I_{Sync.9} = 0.3$ mA		Pin 2	I_I	4.5			mA
C_t–charging current							
$V_S = 13$ V, $V_{I2} = V_{I7} = V_{\varphi 8} = V_{sync9} = 0$ V, $\frac{t_p}{T} = 0.01$, $t_p \leqq 1$ ms		Pin 2	$-I_I$	10		30	mA

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			Min.	Typ.	Max.	
C_s–charging current $V_S = V_{I2} = V_{\varphi 8} = 13$ V, $V_{I7} = V_{sync9} = 0$ V						
$\frac{t_p}{T} = 0.01$, $t_p \leqq 1$ ms	Pin 7	$-I_I$	20		62	mA
Output saturation voltage $V_S = V_{I2} = 16$ V, $V_{I7} = V_{\varphi 8} = 0$ V, $I_{I11} = 50$ µA						
$I_{O10} = 20$ mA, $-I_{sync9} = 0.3$ mA	Pin 10	V_{Osat}		0.3	1.0	V
$I_{O14} = 20$ mA, $I_{sync9} = 0.3$ mA	Pin 14	V_{Osat}		0.3	1.0	V

AC characteristics

$T_{amb} =$ 25 °C, Fig. 3, 4, 6

Rise time	Pin 10	t_r			0.5	µs
	Pin 14	t_r			0.5	ms
Pulse width Fig. 10	Pin 10	t_p	0.1		4	ms
	Pin 14	t_p	0.1		4	ms
Pulse phasing difference for two half-waves $f = 50$ Hz		$\Delta\varphi$			±3°	
Inter IC phasing difference $f = 50$ Hz		$\Delta\varphi$			±3°	
Pulse phasing front limit Fig. 6 $f = 50$ Hz		φ_v	177°			
Pulse phasing rear limit Fig. 6, 9 $f = 50$ Hz		φ_h			0°	

Angle of current flow $\varphi = 0°...177°$ at $V_{\varphi 8} = 0.2...7.5$ V, $\varphi_h = 0°$, Fig. 6, 12

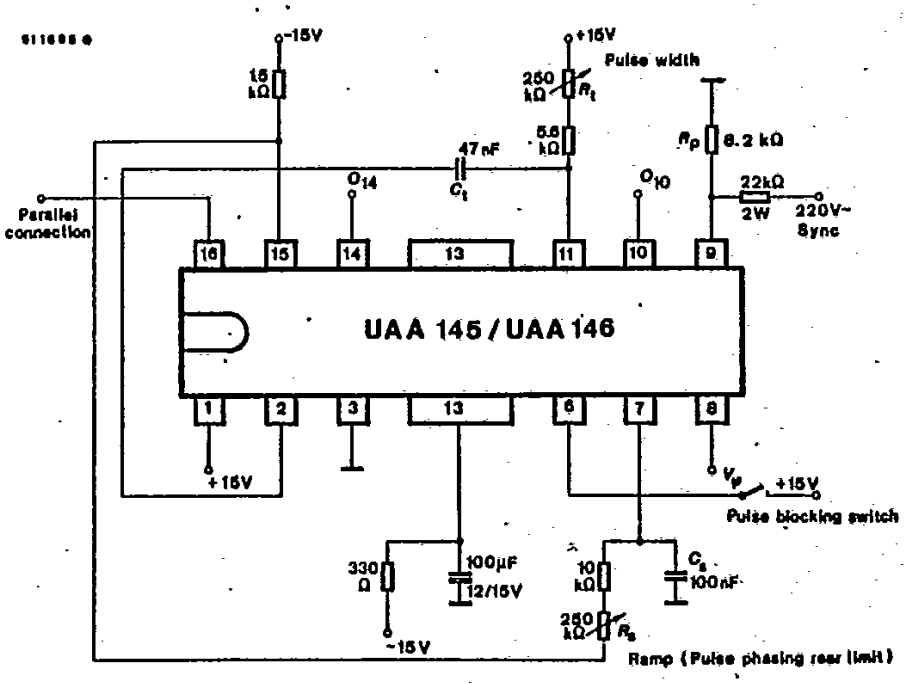


Fig. 4 Test circuit for ac characteristics

Pulse diagram

Fig. 5 shows the pulse voltage waveforms measured at various points of the circuit, all signals being time-referenced to the sync signal shown at the top. The input circuit limits any signal applied to ±0.8 V at Pin 9. The sync pulse can be measured at Pin 16, whereas the ramp waveform and the pulse phasing rear limit (φ_h) at Pin 7. The time relationship between the shift voltage applied to Pin 8 and the ramp waveform are indicated by dotted lines. A pulse trigger signal is produced whenever the ramp crosses the shift level. The memory control pulse can be monitored by means of an oscilloscope applied to Pin 6. The Pin 11 pulse waveform is that at C_t, and the waveforms at Pin 10 and Pin 11 are those of the output pulses.

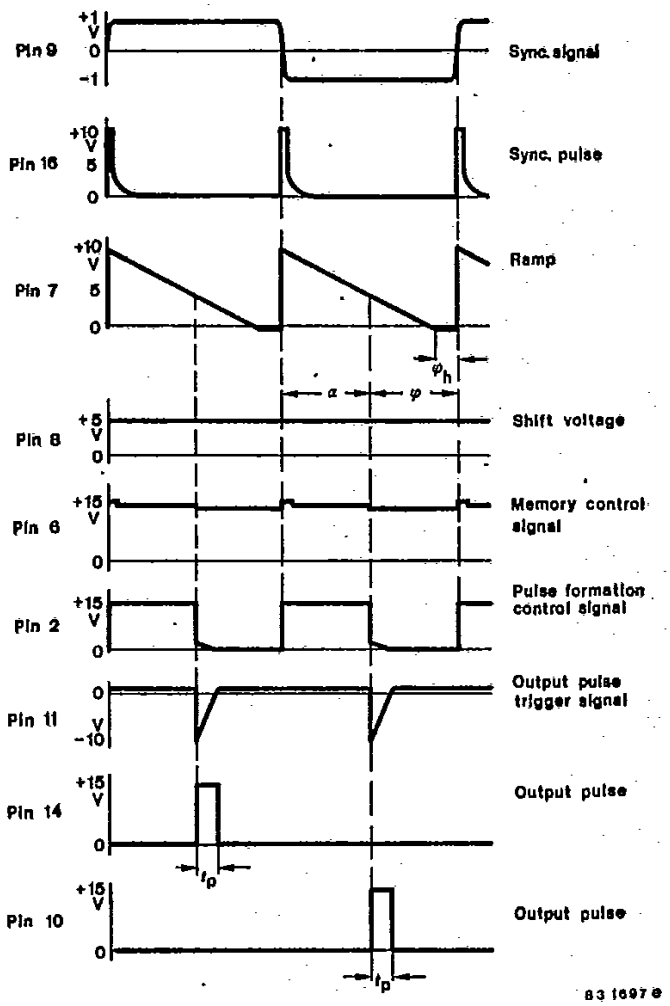


Fig. 5 Pulse diagram

Influence of external components, sync time

An ideal 0 – 180° shift range and perfect half-cycle pulse timing symmetry are attained, if the sync pulse duration is kept short. However, there is a lower pulse duration limit, which is governed by the time required to charge capacitor C_s (Fig. 7).
As can be seen, it takes about 35 µs to charge C_s. The sync time can be altered by adjustment of R_p, the relationship between R_p and the sync time being shown in Fig. 8. The ratio of R and R_p determines the width of internal sync pulse, t_{sync}, at Pin 16. The pulse shape is valid only for sync pulse of 220 V_{ac}. Lower the sync voltage, longer is the sync pulse.
A minimum of 50 µs (max. 200 µs) input sync pulse is required for a pulse symmetry of $\Delta\varphi \leqq \pm 3$ degree.

Pulse phasing limits

The pulse phasing front limit is determined by limiting the maximum shift voltage applied to Pin 8 which is thus adjustable by external circuit. This can be done by connecting a Z-diode between Pin 8 and Pin 3. The pulse phasing rear limit, φ_h, is the residual phase angle of the output pulses when the shift voltage V_φ is zero. Since φ_h coincides with the zero crossover point of the ramp, it can be adjusted by variation of the time constant C_sR_s (Fig. 4). Fig. 9 shows the pulse phasing rear limit plotted as function of R_s.

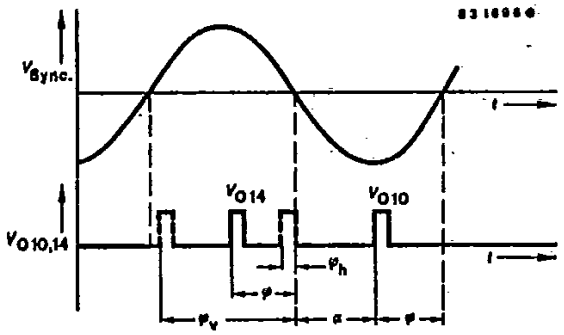


Fig. 6 Pulse phasing

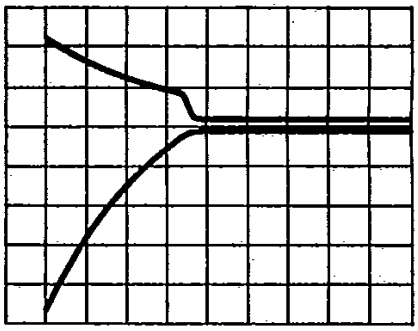
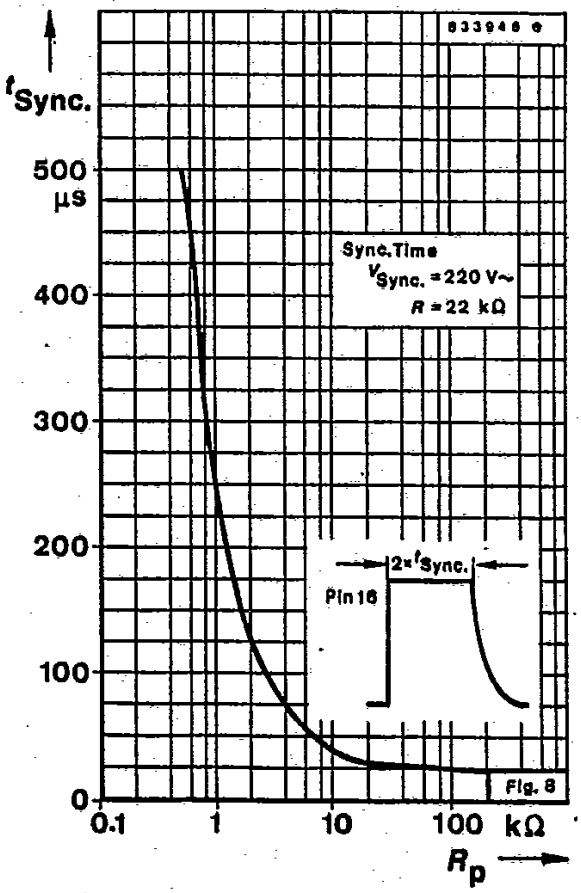


Fig. 7 Charging time 10 µs/div.

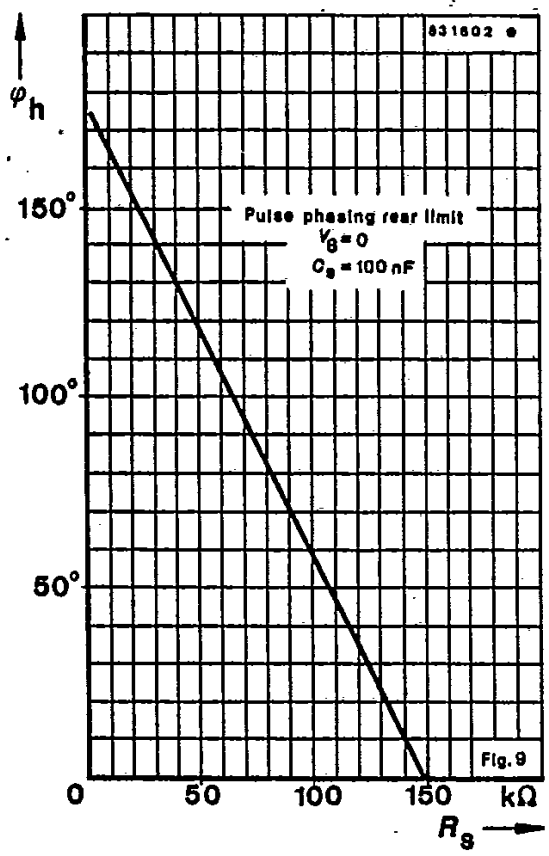


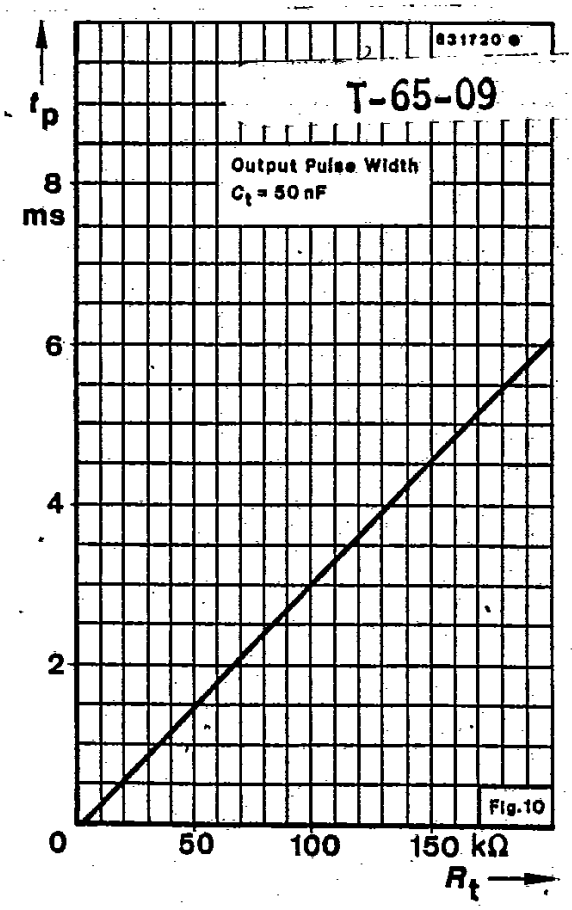
Pulse blocking

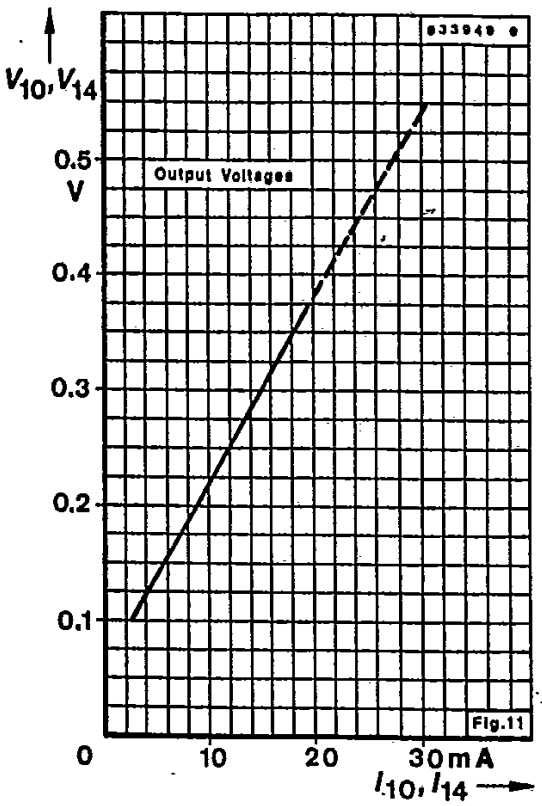
The output pulses can be blocked via Pin 6, the memory content being erased whenever Pin 6 is connected to Pin 1. This effectively de-activates the pulse generator; any output pulse in the process of generation is interrupted.
Pulse blocking can be accomplished either via relay contacts or a PNP switching transistor (Fig. 4)

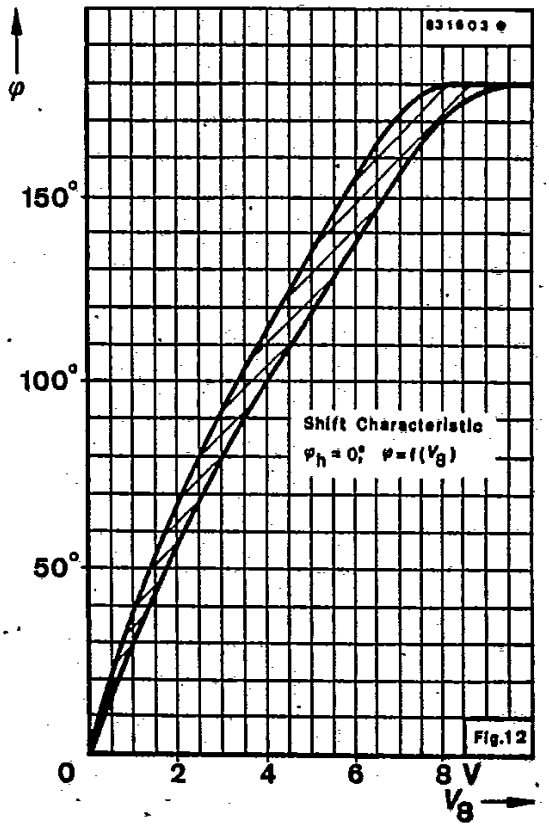
Output pulse width

The output pulse width can be varied by adjustment of R_t and C_t. In Fig. 10 pulse width is shown plotted as a function of R_t for $C_t = 50$ nF.
The output pulse always finishes at zero crossover. This means that if there is a minimum pulse width requirement (for example, when the load is inductive) provision must be made for a corresponding pulse phasing rear limit. The output stages are arranged so that the transistors are cut off when a pulse is produced. Consequently, the thyristor trigger pulse current flows via the external load resistors, this current being passed by the transistors during the period when no output pulse is produced. During this period the output voltage drops to the transistor saturation level and is therefore load dependent. Fig. 11 shows the relationship between saturation voltage and load current.



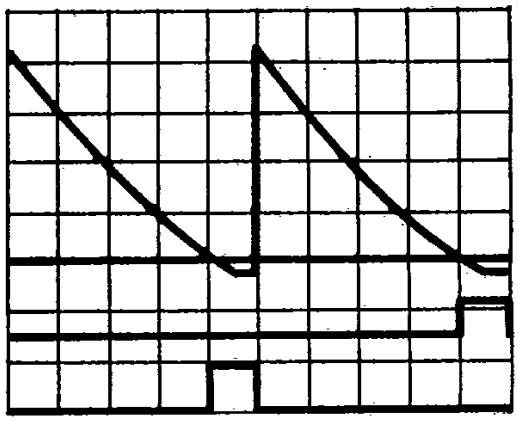






Shift characteristic

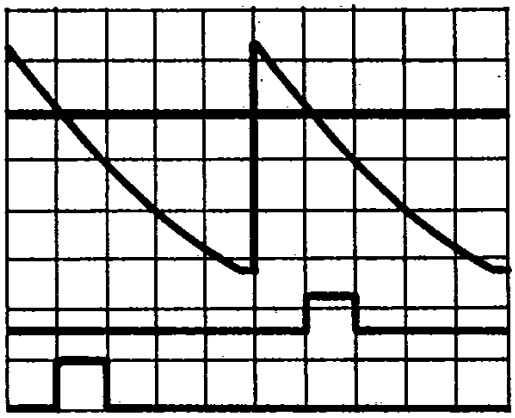
In Fig. 12 the angle of phase shift is shown plotted as a function of the voltage applied to Pin 8 for a pulse phasing rear limit of approximately 0°. Because the ramp waveform is a part of the exponential function, the shift curve is also exponential.
The limitation of the shift voltage to approximately 8.5 V is due to the internal Z-diode Z_4, which has a voltage spread of 7 to 9 V.
The waveforms in Figs. 13...15 show the output pulse phase shift as a function of V_φ. It can be seen from the oscillograms, the instants at which pulses are released coincide with the intersections of the ramp and the shift voltage.



P_7 Ramp 2 V/div

P_8 Ref. voltage 2 V/div
0 V
V_{O14} 20 V/div
0 V
V_{O10} 20 V/div
0 V

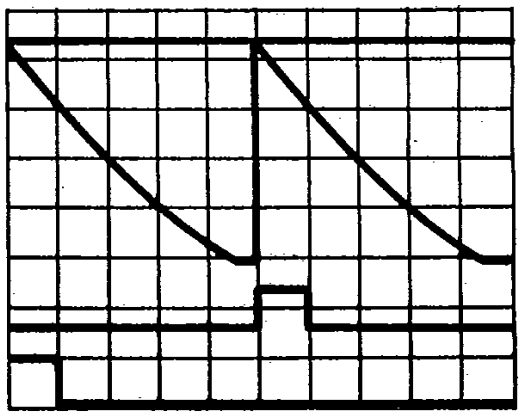
Fig. 13 Output pulses phase shift 2 ms/div



P_8 Ref. voltage 2 V/div
P_7 Ramp 2 V/div

0 V
V_{O14} 20 V/div
0 V
V_{O10} 20 V/div
0 V

Fig. 14 Output pulses phase shift 2 ms/div



P_8 Ref. voltage 2 V/div

P_7 Ramp 2 V/div

0 V
V_{O14} 20 V/div
0 V
V_{O10} 20 V/div
0 V

Fig. 15 Output pulses phase shift 2 ms/div

Applications

Parallel connection for three-phase current applications

T-65-09

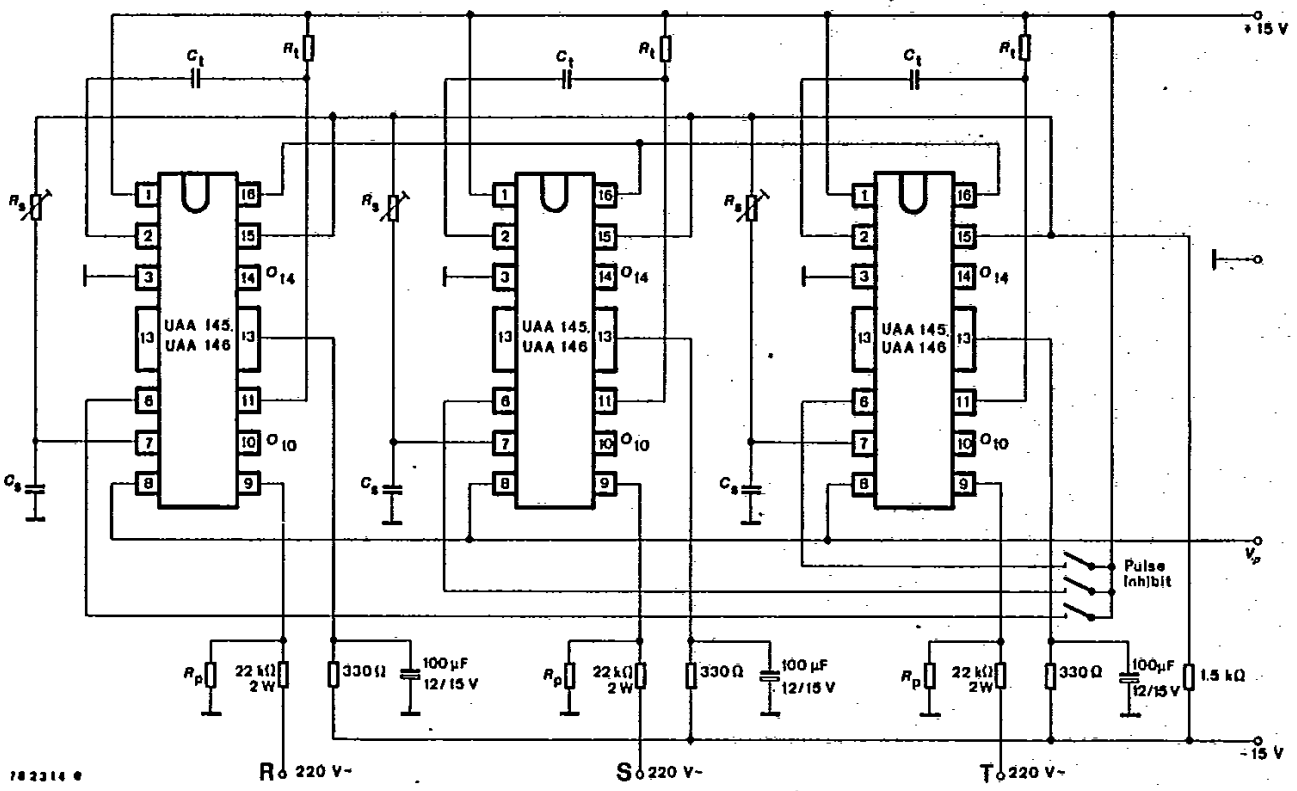
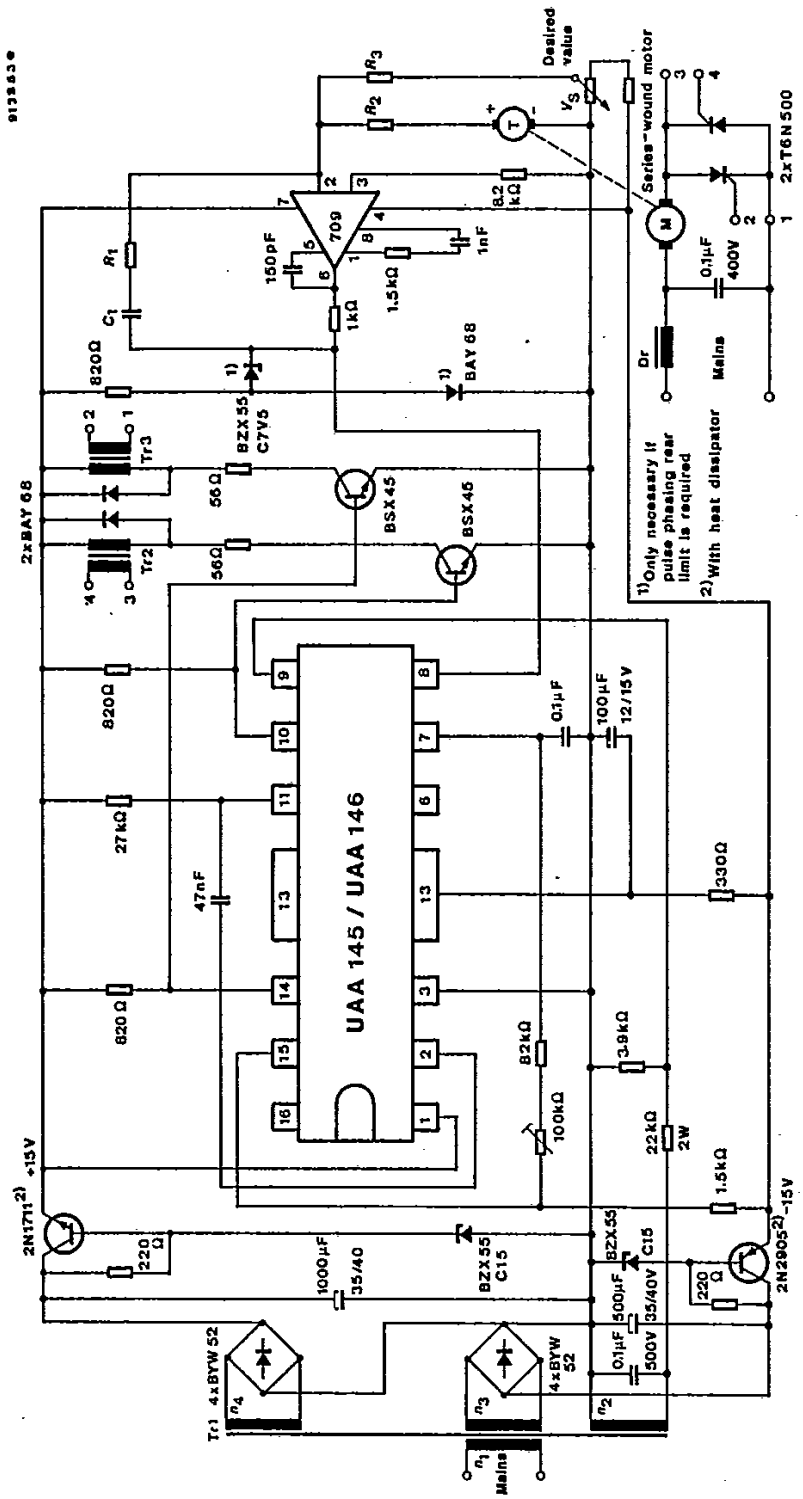


Fig. 17 Parallel connection for three-phase current applications. For polyphase operation connect all Pins 15 and Pins 16.

To ensure good pulse phasing symmetry as well as identical shift characteristics in three-phase applications, when three devices are employed, two parallel connection pins (Fig. 17) are provided on each device. Besides the supply pins, the input pins 15 and 16 are to be paralled. If this is done, then all the Z_4 and Z_3 diodes are connected in parallel so that the reference voltage effective for all three devices becomes that of the Z-diode with the lowest operating voltage. In this way all the C_S capacitors are charged and discharged to the same voltage levels. By symmetrical adjustment of the time constants with resistors R_S, good pulse phasing symmetry and identical shift characteristics are attained.



Tr. 1: Transformer M 55 (DIN...)
n_1 = 2400 turns/0.15 mm dia.
n_2 = 2500 turns/0.1 mm dia.
$n_3 = n_4$ = 200 turns/0.2 mm dia.

Tr. 2; Tr. 3: Pulse transformer
e.g. VAC 407/037-03 PF

Dr.: Interference suppression choke
e.g. VAC FD-6-01-KN
(Vacuumschmelze GmbH, Hanau)

Fig. 18 Speed control with tacho-generator

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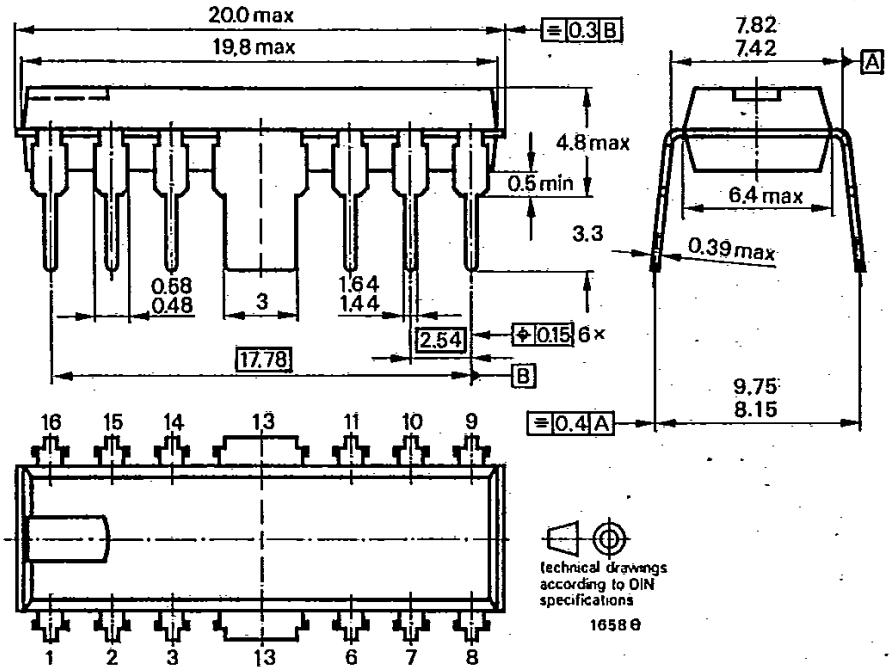
Dimensions in mm

T-65-09



Case:
DIP Special