LMD18245 3A, 55V DMOS Full-Bridge Motor Driver

Check for Samples: LMD18245

FEATURES

- **DMOS Power Stage Rated at 55V and 3A Continuous**
- **Low $R_{DS(ON)}$ of Typically 0.3Ω per Power Switch**
- **Internal Clamp Diodes**
- **Low-loss Current Sensing Method**
- **Digital or Analog Control of Motor Current**
- **TTL and CMOS Compatible Inputs**
- **Thermal Shutdown (Outputs Off) at T_J = 155°C**
- **Overcurrent Protection**
- **No Shoot-Through Currents**
- **15-lead Package**

APPLICATIONS

- **Full, Half and Microstep Stepper Motor Drives**
- **Stepper Motor and Brushed DC Motor Servo Drives**
- **Automated Factory, Medical and Office Equipment**

DESCRIPTION

The LMD18245 full-bridge power amplifier incorporates all the circuit blocks required to drive and control current in a brushed type DC motor or one phase of a bipolar stepper motor. The multi-technology process used to build the device combines bipolar and CMOS control and protection circuitry with DMOS power switches on the same monolithic structure. The LMD18245 controls the motor current via a fixed off-time chopper technique.

An all DMOS H-bridge power stage delivers continuous output currents up to 3A (6A peak) at supply voltages up to 55V. The DMOS power switches feature low $R_{DS(ON)}$ for high efficiency, and a diode intrinsic to the DMOS body structure eliminates the discrete diodes typically required to clamp bipolar power stages.

An innovative current sensing method eliminates the power loss associated with a sense resistor in series with the motor. A four-bit digital-to-analog converter (DAC) provides a digital path for controlling the motor current, and, by extension, simplifies implementation of full, half and microstep stepper motor drives. For higher resolution applications, an external DAC can be used.

Functional Block and Connection Diagram

15-Lead TO-220 Power Package (NDL)

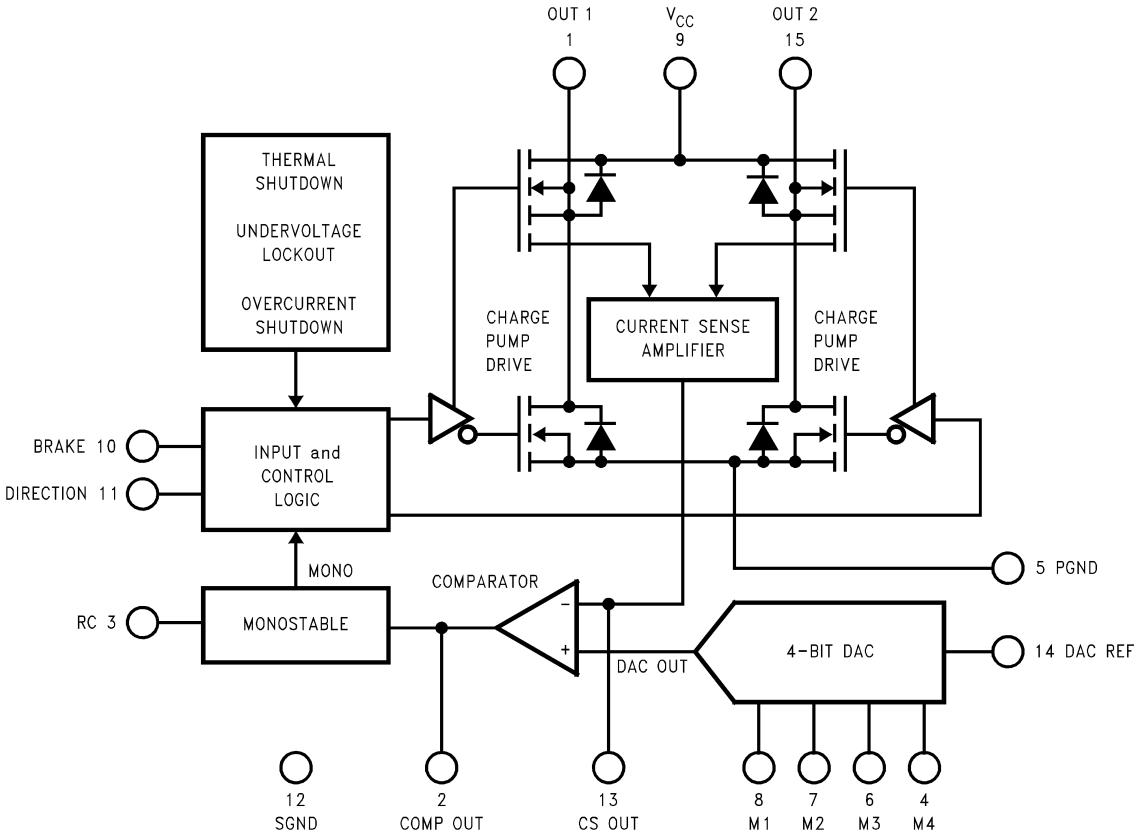

Figure 1. Functional Block Diagram

Connection Diagram

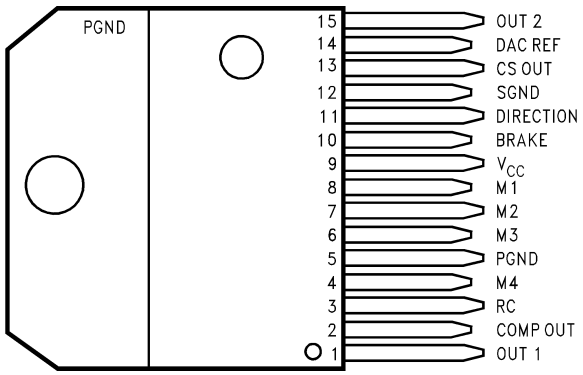

Figure 2. Top View
15-Lead Package TO-220 Power Package
See Package Number NDL0015A

Pinout Descriptions

(See Functional Block and Connection Diagrams)

Pin 1, OUT 1: Output node of the first half H-bridge.

Pin 2, COMP OUT: Output of the comparator. If the voltage at CS OUT exceeds that provided by the DAC, the comparator triggers the monostable.

Pin 3, RC: Monostable timing node. A parallel resistorcapacitor network connected between this node and ground sets the monostable timing pulse at about 1.1 RC seconds.

Pin 5, PGND: Ground return node of the power bridge. Bond wires (internal) connect PGND to the tab of the TO-220 package.

Pins 4 and 6 through 8, M4 through M1: Digital inputs of the DAC. These inputs make up a four-bit binary number with M4 as the most significant bit or MSB. The DAC provides an analog voltage directly proportional to the binary number applied at M4 through M1.

Pin 9, V_{CC}: Power supply node.

Pin 10, BRAKE: Brake logic input. Pulling the BRAKE input logic-high activates both sourcing switches of the power bridge — effectively shorting the load. See SWITCH CONTROL LOGIC TRUTH TABLE(1). Shorting the load in this manner forces the load current to recirculate and decay to zero.

Pin 11, DIRECTION: Direction logic input. The logic level at this input dictates the direction of current flow in the load. See SWITCH CONTROL LOGIC TRUTH TABLE(1).

Pin 12, SGND: Ground return node of all signal level circuits.

Pin 13, CS OUT: Output of the current sense amplifier. The current sense amplifier sources 250 µA (typical) per ampere of total forward current conducted by the upper two switches of the power bridge.

Pin 14, DAC REF: Voltage reference input of the DAC. The DAC provides an analog voltage equal to $V_{DAC\ REF} \times D/16$, where D is the decimal equivalent (0–15) of the binary number applied at M4 through M1.

Pin 15, OUT 2: Output node of the second half H-bridge.

SWITCH CONTROL LOGIC TRUTH TABLE(1)

BRAKE	DIRECTION	MONO	Active Switches
H	X	X	Source 1, Source 2
L	H	L	Source 2
L	H	H	Source 2, Sink 1
L	L	L	Source 1
L	L	H	Source 1, Sink 2

(1) X = don't care. MONO is the output of the monostable.
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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

DC Voltage at:	
OUT 1, V_{CC}, and OUT 2	+60V
COMP OUT, RC, M4, M3, M2, M1, BRAKE,	+12V
DIRECTION, CS OUT, and DAC REF	
DC Voltage PGND to SGND	±400mV
Continuous Load Current	3A
Peak Load Current (3)	6A
Junction Temperature ($T_{J(max)}$)	+150°C
Power Dissipation (4) :	
TO-220 (T_A = 25°C, Infinite Heatsink)	25W
TO-220 (T_A = 25°C, Free Air)	3.5W
ESD Susceptibility (5)	1500V
Storage Temperature Range (T_S)	−40°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside the rated Operating Conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Unless otherwise stated, load currents are pulses with widths less than 2 ms and duty cycles less than 5%.
(4) The maximum allowable power dissipation at any ambient temperature is $P_{Max} = (125 - T_A)/\theta_{JA}$, where 125°C is the maximum junction temperature for operation, T_A is the ambient temperature in °C, and $\theta_{JA}$is the junction-to-ambient thermal resistance in °C/W. Exceeding P_{max} voids the Electrical Specifications by forcing $T_J$above 125°C. If the junction temperature exceeds 155°C, internal circuitry disables the power bridge. When a heatsink is used, $\theta_{JA}$is the sum of the junction-to-case thermal resistance of the package, θ_{JC}, and the case-to-ambient thermal resistance of the heatsink.
(5) ESD rating is based on the human body model of 100 pF discharged through a 1.5 kΩ resistor. M1, M2, M3 and M4, pins 8, 7, 6 and 4 are protected to 800V.

Operating Conditions (1)

Temperature Range (T_J) (2)	−40°C to +125°C
Supply Voltage Range (V_{CC})	+12V to +55V
CS OUT Voltage Range	0V to +5V
DAC REF Voltage Range	0V to +5V
MONOSTABLE Pulse Range	10 µs to 100 ms

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device outside the rated Operating Conditions.
(2) The maximum allowable power dissipation at any ambient temperature is $P_{Max} = (125 - T_A)/\theta_{JA}$, where 125°C is the maximum junction temperature for operation, T_A is the ambient temperature in °C, and $\theta_{JA}$is the junction-to-ambient thermal resistance in °C/W. Exceeding P_{max} voids the Electrical Specifications by forcing $T_J$above 125°C. If the junction temperature exceeds 155°C, internal circuitry disables the power bridge. When a heatsink is used, $\theta_{JA}$is the sum of the junction-to-case thermal resistance of the package, θ_{JC}, and the case-to-ambient thermal resistance of the heatsink.

Electrical Characteristics (1)

The following specifications apply for V_{CC} = +42V, unless otherwise stated. **Boldface limits apply over the operating temperature range, −40°C ≤ T_J ≤ +125°C.** All other limits apply for T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (2)	Limit (2)	Units (Limits)
I_{CC}	Quiescent Supply Current	DAC REF = 0V, V_{CC} = +20V	8		mA
				15	mA (max)
POWER OUTPUT STAGE					
$R_{DS(ON)}$	Switch ON Resistance	I_{LOAD} = 3A	0.3	0.4	Ω (max)
				0.6	Ω (max)
		I_{LOAD} = 6A	0.3	0.4	Ω (max)
				0.6	Ω (max)
V_{DIODE}	Body Diode Forward Voltage	I_{DIODE} = 3A	1.0		V
				1.5	V(max)
T_{rr}	Diode Reverse Recovery Time	I_{DIODE} = 1A	80		ns
Q_{rr}	Diode Reverse Recovery Charge	I_{DIODE} = 1A	40		nC
$t_{D(ON)}$	Output Turn ON Delay Time				
	Sourcing Outputs	I_{LOAD} = 3A	5		µs
	Sinking Outputs	I_{LOAD} = 3A	900		ns
$t_{D(OFF)}$	Output Turn OFF Delay Time				
	Sourcing Outputs	I_{LOAD} = 3A	600		ns
	Sinking Outputs	I_{LOAD} = 3A	400		ns
t_{ON}	Output Turn ON Switching Time				
	Sourcing Outputs	I_{LOAD} = 3A	40		µs
	Sinking Outputs	I_{LOAD} = 3A	1		µs
t_{OFF}	Output Turn OFF Switching Time				
	Sourcing Outputs	I_{LOAD} = 3A	200		ns
	Sinking Outputs	I_{LOAD} = 3A	80		ns
t_{pw}	Minimum Input Pulse Width	Pins 10 and 11	2		µs
t_{DB}	Minimum Dead Band	(3)	40		ns
CURRENT SENSE AMPLIFIER					
	Current Sense Output	I_{LOAD} = 1A (4)		200	µA (min)
			250	**175**	µA (min)
				300	µA (max)
				325	µA (max)
	Current Sense Linearity Error	0.5A ≤ I_{LOAD} ≤ 3A (4)	±6		%
				±9	%(max)
	Current Sense Offset	I_{LOAD} = 0A	5		µA
				20	µA (max)

(1) Unless otherwise stated, load currents are pulses with widths less than 2 ms and duty cycles less than 5%.
(2) All limits are 100% production tested at 25°C. Temperature extreme limits are ensured via correlation using accepted SQC (Statistical Quality Control) methods. All limits are used to calculate AOQL (Average Outgoing Quality Level). Typicals are at T_J = 25°C and represent the most likely parametric norm.
(3) Asymmetric turn OFF and ON delay times and switching times ensure a switch turns OFF before the other switch in the same half H-bridge begins to turn ON (preventing momentary short circuits between the power supply and ground). The transitional period during which both switches are OFF is commonly referred to as the dead band.
(4) (I_{LOAD}, I_{SENSE}) data points are taken for load currents of 0.5A, 1A, 2A and 3A. The current sense gain is specified as I_{SENSE}/I_{LOAD} for the 1A data point. The current sense linearity is specified as the slope of the line between the 0.5A and 1A data points minus the slope of the line between the 2A and 3A data points all divided by the slope of the line between the 0.5A and 1A data points.

Electrical Characteristics [1] (continued)

The following specifications apply for V_{CC} = +42V, unless otherwise stated. **Boldface limits apply over the operating temperature range, −40°C ≤ T_J ≤ +125°C.** All other limits apply for T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical [2]	Limit [2]	Units (Limits)
DIGITAL-TO-ANALOG CONVERTER (DAC)					
	Resolution			**4**	Bits (min)
	Monotonicity			**4**	Bits (min)
	Total Unadjusted Error		0.125	0.25 **0.5**	LSB (max) LSB (max)
	Propagation Delay		50		ns
I_{REF}	DAC REF Input Current	DAC REF = +5V	−0.5	 **±10**	µA µA (max)
COMPARATOR AND MONOSTABLE					
	Comparator High Output Level		6.27		V
	Comparator Low Output Level		88		mV
	Comparator Output Current Source Sink		 0.2 3.2		 mA mA
t_{DELAY}	Monostable Turn OFF Delay	[5]	1.2	 2.0	µs µs (max)
PROTECTION AND PACKAGE THERMAL RESISTANCES					
	Undervoltage Lockout, V_{CC}			5 8	V (min) V (max)
T_{JSD}	Shutdown Temperature, T_J		155		°C
	Package Thermal Resistances				
θ_{JC}	Junction-to-Case, TO-220		1.5		°C/W
θ_{JA}	Junction-to-Ambient, TO-220		35		°C/W
LOGIC INPUTS					
V_{IL}	Low Level Input Voltage			**−0.1** **0.8**	V (min) V (max)
V_{IH}	High Level Input Voltage			**2** **12**	V (min) V (max)
I_{IN}	Input Current	V_{IN} = 0V or 12V		**±10**	µA (max)

(5) Turn OFF delay, t_{DELAY}, is defined as the time from the voltage at the output of the current sense amplifier reaching the DAC output voltage to the lower DMOS switch beginning to turn OFF. With V_{CC} = 32V, DIRECTION high, and 200Ω connected between OUT1 and V_{CC}, the voltage at RC is increased from 0V to 5V at 1.2V/µs, and t_{DELAY} is measured as the time from the voltage at RC reaching 2V to the time the voltage at OUT 1 reaches 3V.

Typical Performance Characteristics

RDS(ON) vs Temperature

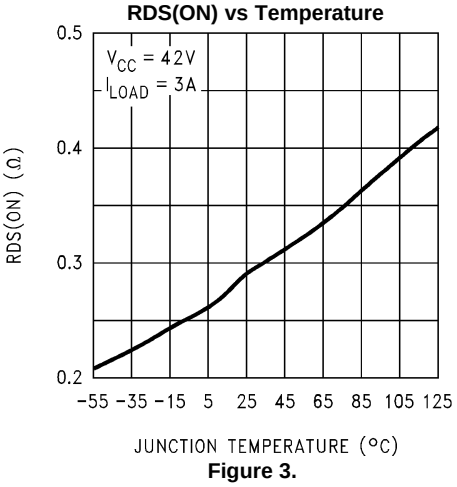


Figure 3.

RDS(ON) vs Load Current

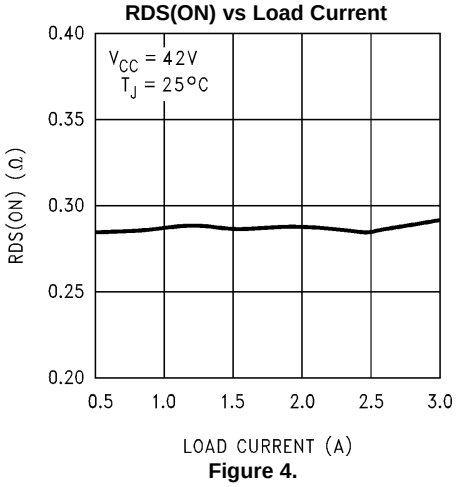


Figure 4.

RDS(ON) vs Supply Voltage

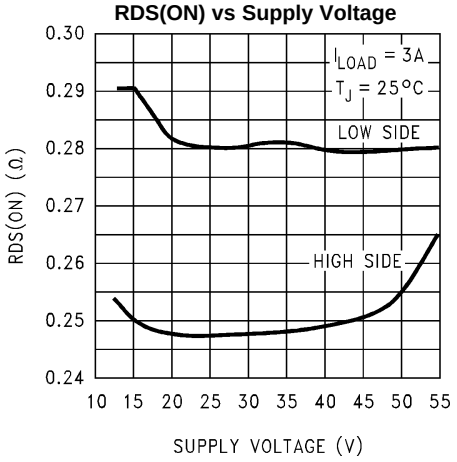


Figure 5.

Current Sense Output vs Load Current

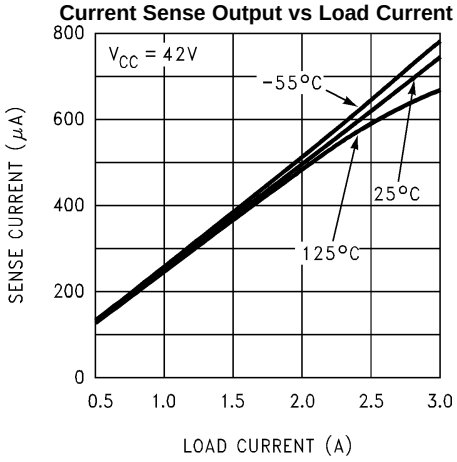


Figure 6.

Supply Current vs Supply Voltage

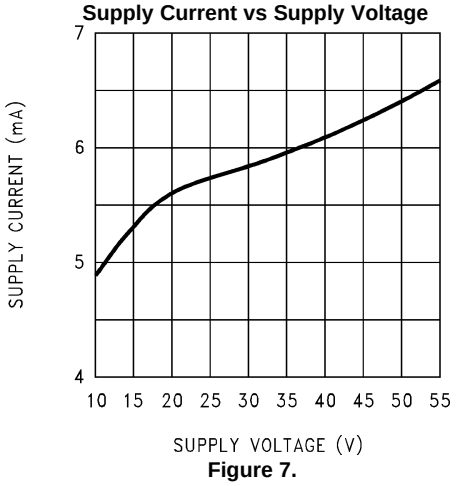


Figure 7.

Supply Current vs Temperature

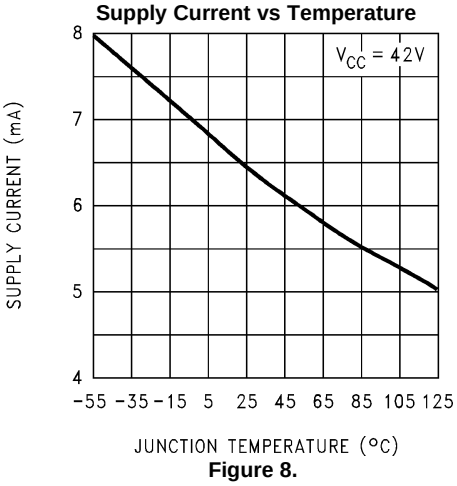
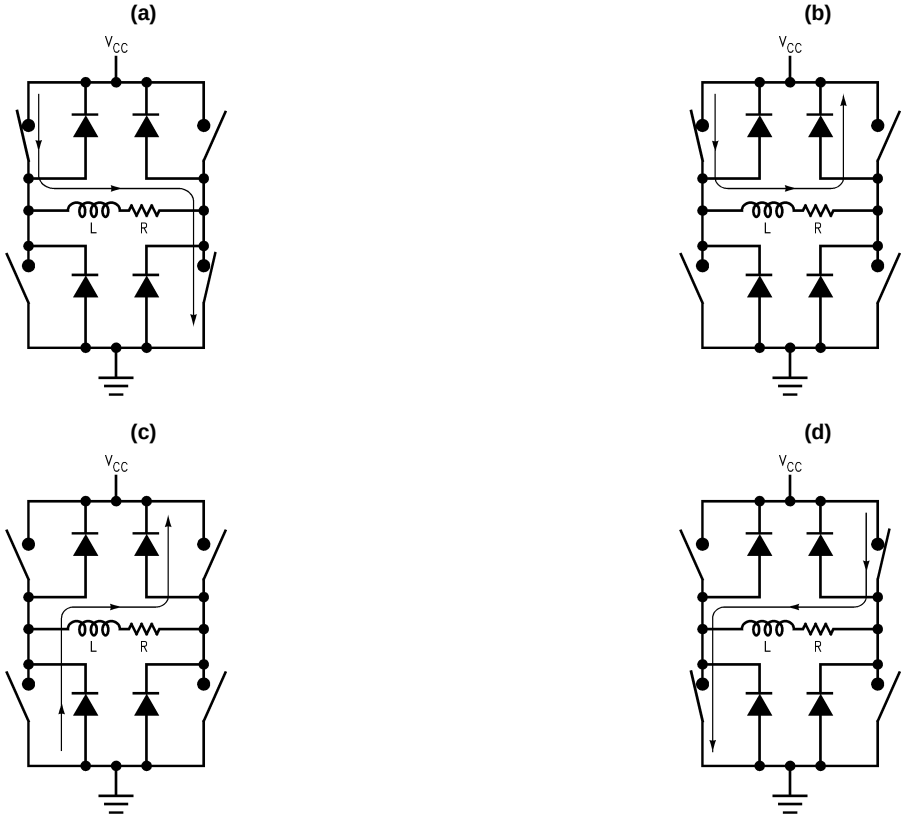


Figure 8.

FUNCTIONAL DESCRIPTIONS

TYPICAL OPERATION OF A CHOPPER AMPLIFIER

Chopper amplifiers employ feedback driven switching of a power bridge to control and limit current in the winding of a motor (Figure 9). The bridge consists of four solid state power switches and four diodes connected in an H configuration. Control circuitry (not shown) monitors the winding current and compares it to a threshold. While the winding current remains less than the threshold, a source switch and a sink switch in opposite halves of the bridge force the supply voltage across the winding, and the winding current increases rapidly towards V_{CC}/R (Figure 9*a* and Figure 9*d*). As the winding current surpasses the threshold, the control circuitry turns OFF the sink switch for a fixed period or *off-time.* During the off-time, the source switch and the opposite upper diode short the winding, and the winding current recirculates and decays slowly towards zero (Figure 9*b* and Figure 9*e*). At the end of the off-time, the control circuitry turns back ON the sink switch, and the winding current again increases rapidly towards V_{CC}/R (Figure 9*a* and Figure 9*d* again). The above sequence repeats to provide a current chopping action that limits the winding current to the threshold (Figure 9*g*). Chopping only occurs if the winding current reaches the threshold. During a change in the direction of the winding current, the diodes provide a decay path for the initial winding current (Figure 9*c* and Figure 9*f*). Since the bridge shorts the winding for a fixed period, this type of chopper amplifier is commonly referred to as a *fixed off-time chopper.*



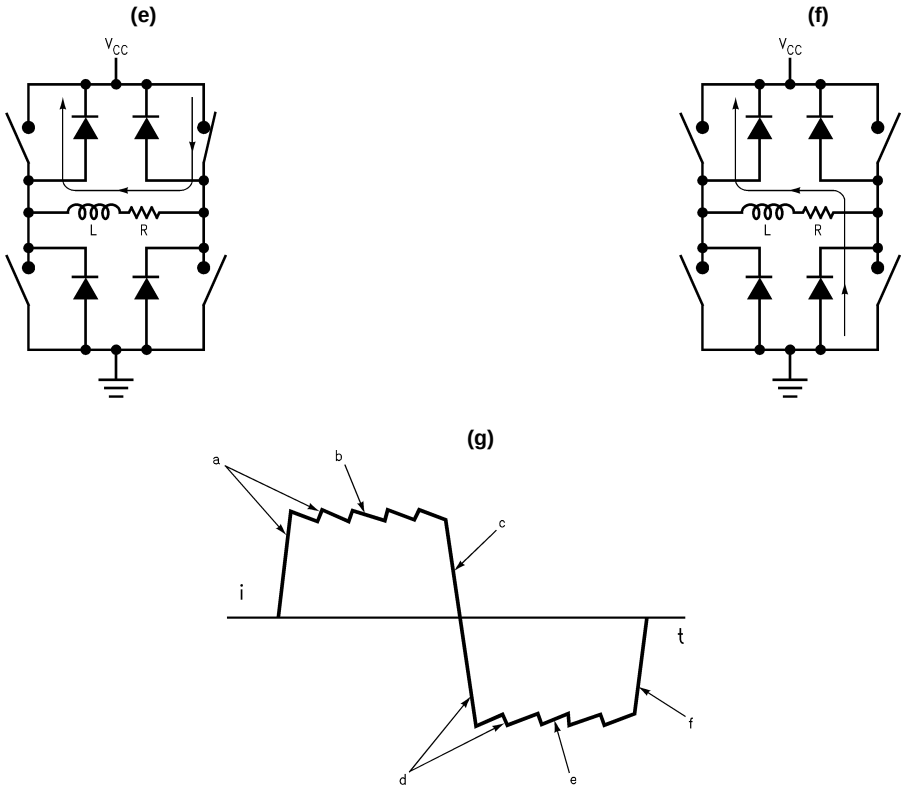


Figure 9. Chopper Amplifier Chopping States: Full V_{CC} Applied Across the Winding (a) and (d), Shorted Winding (b) and (e), Winding Current Decays During a Change in the Direction of the Winding Current (c) and (f), and the Chopped Winding Current (g)

THE LMD18245 CHOPPER AMPLIFIER

The LMD18245 incorporates all the circuit blocks needed to implement a fixed off-time chopper amplifier. These blocks include: an all DMOS, full H-bridge with clamp diodes, an amplifier for sensing the load current, a comparator, a monostable, and a DAC for digital control of the chopping threshold. Also incorporated are logic, level shifting and drive blocks for digital control of the direction of the load current and braking.

THE H-BRIDGE

The power stage consists of four DMOS power switches and associated body diodes connected in an H-bridge configuration (Figure 10).

The time constant to charge or discharge any inductor, in this case the motor windings, is defined as:

$$\tau = L/R \quad (1)$$

where

- L is the winding inductance
- R is the sum of the series resistance in the current path including the winding resistance

Turning ON a source switch and a sink switch in opposite halves of the bridge forces the full supply voltage less the switch drops ($I \times R_{DS(ON)}$) across the motor winding. While the bridge remains in this state, the winding current increases exponentially towards a limit dictated by the supply voltage, the switch drops ($I \times R_{DS(ON)}$), and the winding resistance. However, the winding current exponential rate of increase will end when the current chopping circuitry becomes active.

Subsequently turning OFF the sink switch causes a voltage transient that forward biases the body diode of the other source switch. The diode clamps the transient at one diode drop above the supply voltage and provides an alternative current path. While the bridge remains in this state, it essentially shorts the winding, the winding current recirculates and decays exponentially towards zero at a rate that is defined by the L/R time constant.

During a change in the direction of the winding current, both the switches and the body diodes provide a decay path for the initial winding current (Figure 11).

During actual motor operation there are many variables that can effect the motor winding magnetic behavior and performance. Resonance, eddy currents, friction, motor loading, damping, temperature coefficients of the windings, are only a few. These are all issues that are beyond the scope of the this data sheet.

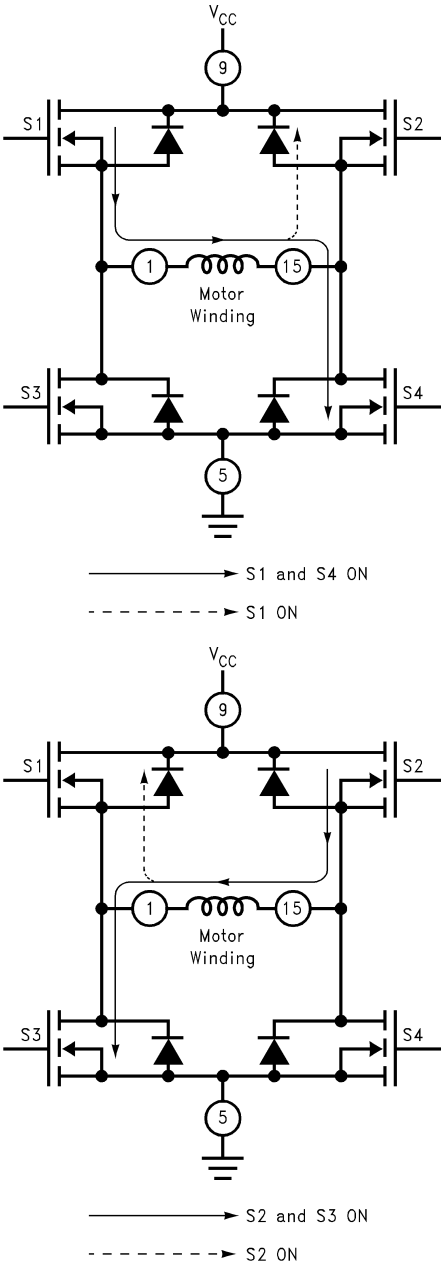


Figure 10. The DMOS H-Bridge

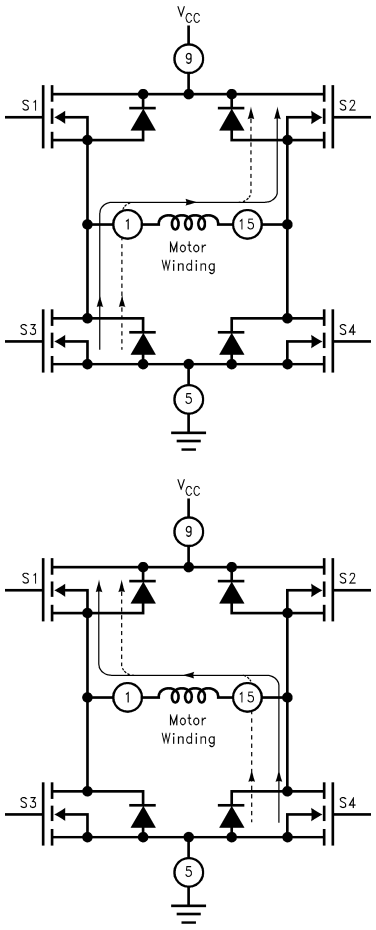


Figure 11. Decay Paths for Initial Winding Current During a Change in the Direction of the Winding Current

THE CURRENT SENSE AMPLIFIER

Many transistor cells in parallel make up the DMOS power switches. The current sense amplifier (Figure 12) uses a small fraction of the cells of both upper switches to provide a unique, low-loss means for sensing the load current. In practice, each upper switch functions as a 1x sense device in parallel with a 4000x power device. The current sense amplifier forces the voltage at the source of the sense device to equal that at the source of the power device; thus, the devices share the total drain current in proportion to the 1:4000 cell ratio. Only the current flowing from drain to source, the forward current, registers at the output of the current sense amplifier. The current sense amplifier, therefore, sources 250 µA per ampere of total forward current conducted by the upper two switches of the power bridge.

The sense current develops a potential across $R_S$that is proportional to the load current; for example, per ampere of load current, the sense current develops one volt across a 4 kΩ resistor (the product of 250 µA per ampere and 4 kΩ). Since chopping of the load current occurs as the voltage at CS OUT surpasses the threshold (the DAC output voltage), R_S sets the gain of the chopper amplifier; for example, a 2 kΩ resistor sets the gain at two amperes of load current per volt of the threshold (the reciprocal of the product of 250 µA per ampere and 2 kΩ). A quarter watt resistor suffices. A low value capacitor connected in parallel with R_S filters the effects of switching noise from the current sense signal.

While the specified maximum DC voltage compliance at CS OUT is 12V, the specified operating voltage range at CS OUT is 0V to 5V.

THE DIGITAL-TO-ANALOG CONVERTER (DAC)

The DAC sets the threshold voltage for chopping at $V_{DAC\ REF}$ × D/16, where D is the decimal equivalent (0–15) of the binary number applied at M4 through M1, the digital inputs of the DAC. M4 is the MSB or most significant bit. For applications that require higher resolution, an external DAC can drive the DAC REF input. While the specified maximum DC voltage compliance at DAC REF is 12V, the specified operating voltage range at DAC REF is 0V to 5V.

THE COMPARATOR, MONOSTABLE AND WINDING CURRENT THRESHOLD FOR CHOPPING

As the voltage at CS OUT surpasses that at the output of the DAC, the comparator triggers the monostable, and the monostable, once triggered, provides a timing pulse to the control logic. During the timing pulse, the power bridge shorts the motor winding, causing current in the winding to recirculate and decay slowly towards zero (Figure 9*b* and Figure 9*e* again). A parallel resistor-capacitor network connected between RC (pin #3) and ground sets the timing pulse or off-time at about 1.1 RC seconds.

Chopping of the winding current occurs as the voltage at CS OUT exceeds that at the output of the DAC; so chopping occurs at a winding current threshold of about

$$(V_{DAC\ REF} \times D/16) \div ((250 \times 10^{-6}) \times R_S)) \text{ amperes.} \quad (2)$$

The R_S value required to set the winding current threshold at the maximum rated current of the LMD18245, with D = 15 and $V_{DAC\ REF}$ of 5.00V would be:

$$(5.00V \times 15/16) \div ((250 \times 10^{-6}) \times 6.25\ k\Omega)) = 3.00A \quad (3)$$

The resulting typical DAC programmable current limit values, for different values of R_S, would be:

Table 1. D to A winding current thresholds for $V_{REF\ DAC}$ = 5.00V

D	R_S = 18.75 kΩ	R_S = 9.375kΩ	R_S = 6.250 kΩ
0	0.00A	0.00A	0.00A
1	0.07A	0.13A	0.20A
2	0.13A	0.27A	0.40A
3	0.20A	0.40A	0.60A
4	0.27A	0.53A	0.80A
5	0.33A	0.67A	1.00A
6	0.40A	0.80A	1.20A
7	0.47A	0.93A	1.40A
8	0.53A	1.07A	1.60A
9	0.60A	1.20A	1.80A
10	0.67A	1.33A	2.00A
11	0.73A	1.47A	2.20A
12	0.80A	1.60A	2.40A
13	0.87A	1.73A	2.60A
14	0.93A	1.87A	2.80A
15	1.00A	2.00A	3.00A

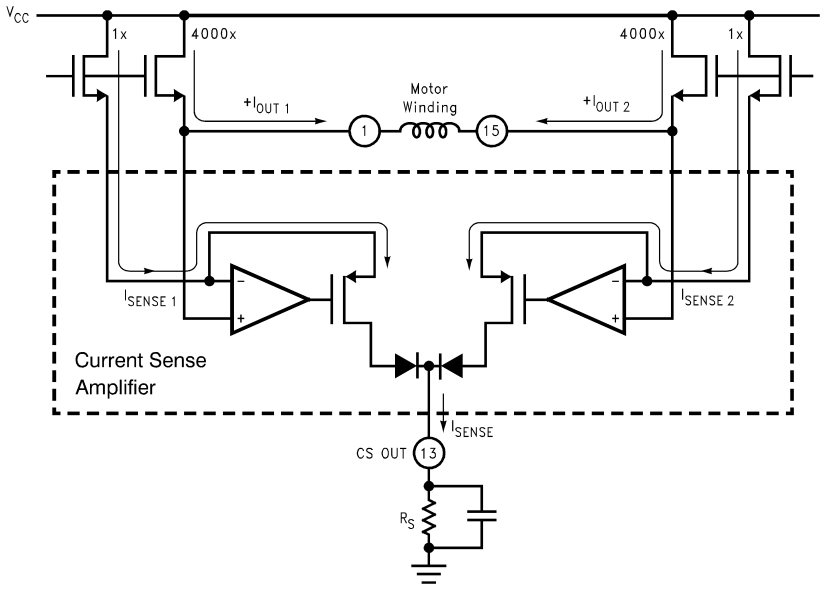


Figure 12. The Source Switches of the Power Bridge and the Current Sense Amplifier

Applications Information

POWER SUPPLY BYPASSING

Step changes in current drawn from the power supply occur repeatedly during normal operation and may cause large voltage spikes across inductance in the power supply line. Care must be taken to limit voltage spikes at V_{CC} to less than the 60V Absolute Maximum Rating. At a change in the direction of the load current, the initial load current tends to raise the voltage at the power supply rail (Figure 11) again. Current transients caused by the reverse recovery of the clamp diodes tend to pull down the voltage at the power supply rail.

Bypassing the power supply line at V_{CC} is required to protect the device and minimize the adverse effects of normal operation on the power supply rail. Using both a 1 µF high frequency ceramic capacitor and a large-value aluminum electrolytic capacitor is highly recommended. A value of 100 µF per ampere of load current usually suffices for the aluminum electrolytic capacitor. Both capacitors should have short leads and be located within one half inch of V_{CC}.

OVERCURRENT PROTECTION

If the forward current in either source switch exceeds a 12A threshold, internal circuitry disables both source switches, forcing a rapid decay of the fault current (Figure 13). Approximately 3 µs after the fault current reaches zero, the device restarts. Automatic restart allows an immediate return to normal operation once the fault condition has been removed. If the fault persists, the device will begin cycling into and out of thermal shutdown. Switching large fault currents may cause potentially destructive voltage spikes across inductance in the power supply line; therefore, the power supply line must be properly bypassed at V_{CC} for the motor driver to survive an extended overcurrent fault.

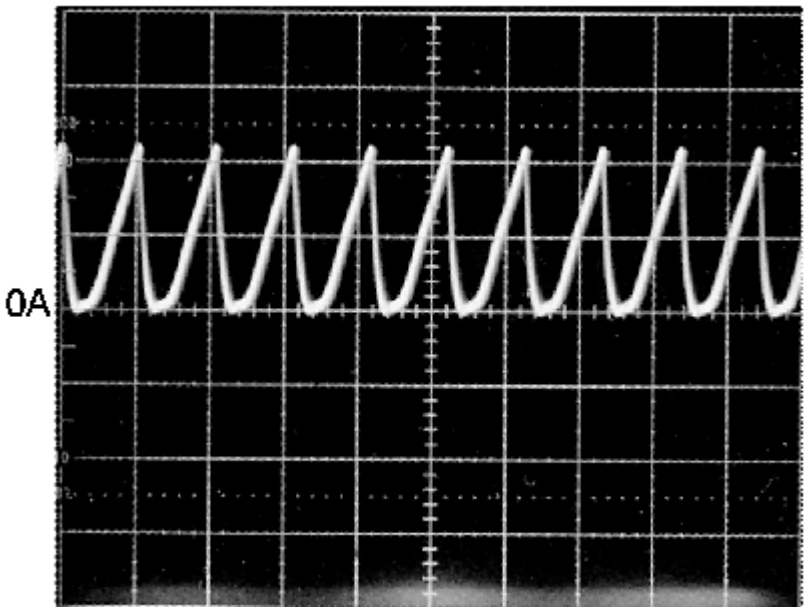
In the case of a locked rotor, the inductance of the winding tends to limit the rate of change of the fault current to a value easily handled by the protection circuitry. In the case of a low inductance short from either output to ground or between outputs, the fault current could surge past the 12A shutdown threshold, forcing the device to dissipate a substantial amount of power for the brief period required to disable the source switches. Because the fault power must be dissipated by only one source switch, a short from output to ground represents the worst case fault. Any overcurrent fault is potentially destructive, especially while operating with high supply voltages (≥30V), so precautions are in order. Sinking V_{CC} for heat with 1 square inch of 1 ounce copper on the printed circuit board is highly recommended. The sink switches are not internally protected against shorts to V_{CC}.

THERMAL SHUTDOWN

Internal circuitry senses the junction temperature near the power bridge and disables the bridge if the junction temperature exceeds about 155°C. When the junction temperature cools past the shutdown threshold (lowered by a slight hysteresis), the device automatically restarts.

UNDERVOLTAGE LOCKOUT

Internal circuitry disables the power bridge if the power supply voltage drops below a rough threshold between 8V and 5V. Should the power supply voltage then exceed the threshold, the device automatically restarts.



Trace: Fault Current at 5A/div
Horizontal: 20 µs/div

Figure 13. Fault Current with V_{CC} = 30V, OUT 1 Shorted to OUT 2, and CS OUT Grounded

The Typical Application

Figure 14 shows the typical application, the power stage of a chopper drive for bipolar stepper motors. The 20 kΩ resistor and 2.2 nF capacitor connected between RC and ground set the off-time at about 48 µs, and the 20 kΩ resistor connected between CS OUT and ground sets the gain at about 200 mA per volt of the threshold for chopping. Digital signals control the thresholds for chopping, the directions of the winding currents, and, by extension, the drive type (full step, half step, etc.). A µprocessor or µcontroller usually provides the digital control signals.

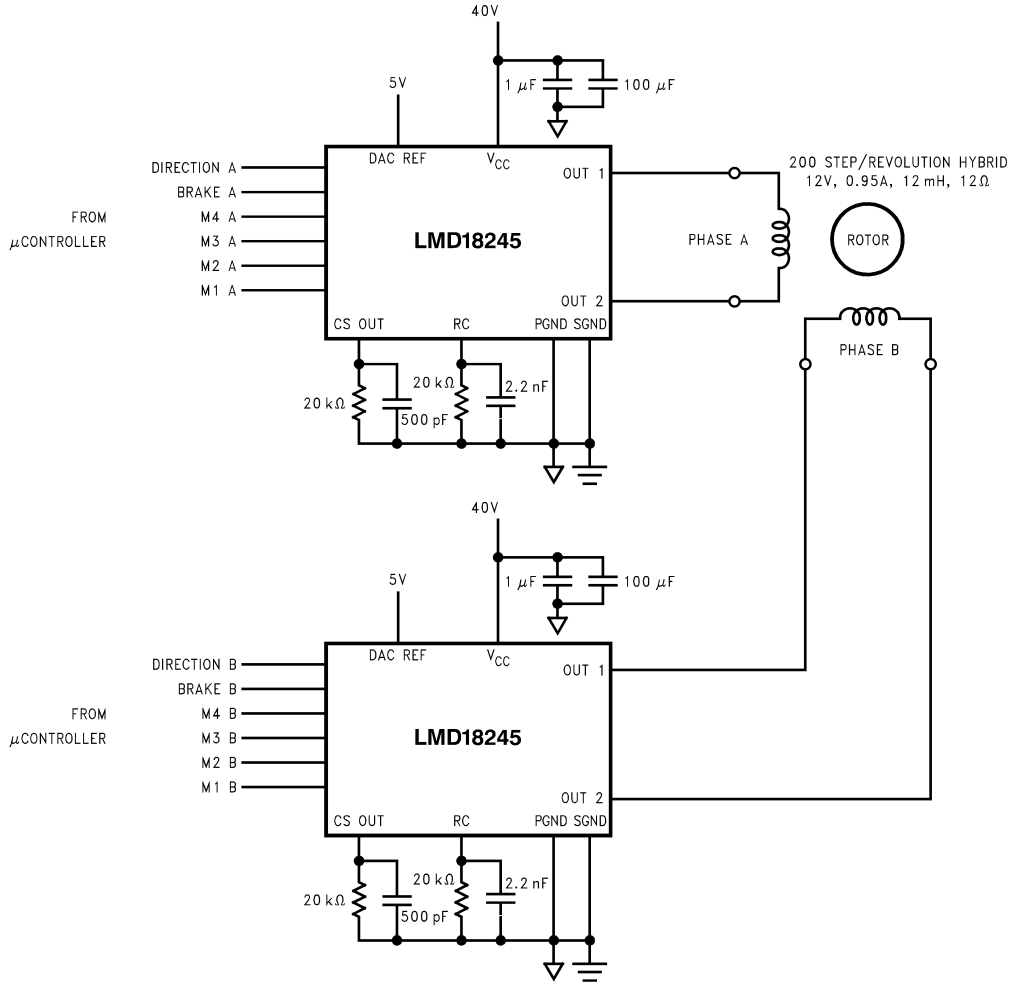


Figure 14. Typical Application Circuit for Driving Bipolar Stepper Motors

ONE-PHASE-ON FULL STEP DRIVE (WAVE DRIVE)

To make the motor take full steps, windings A and B can be energized in the sequence

A→B→A*→B*→A→ …,

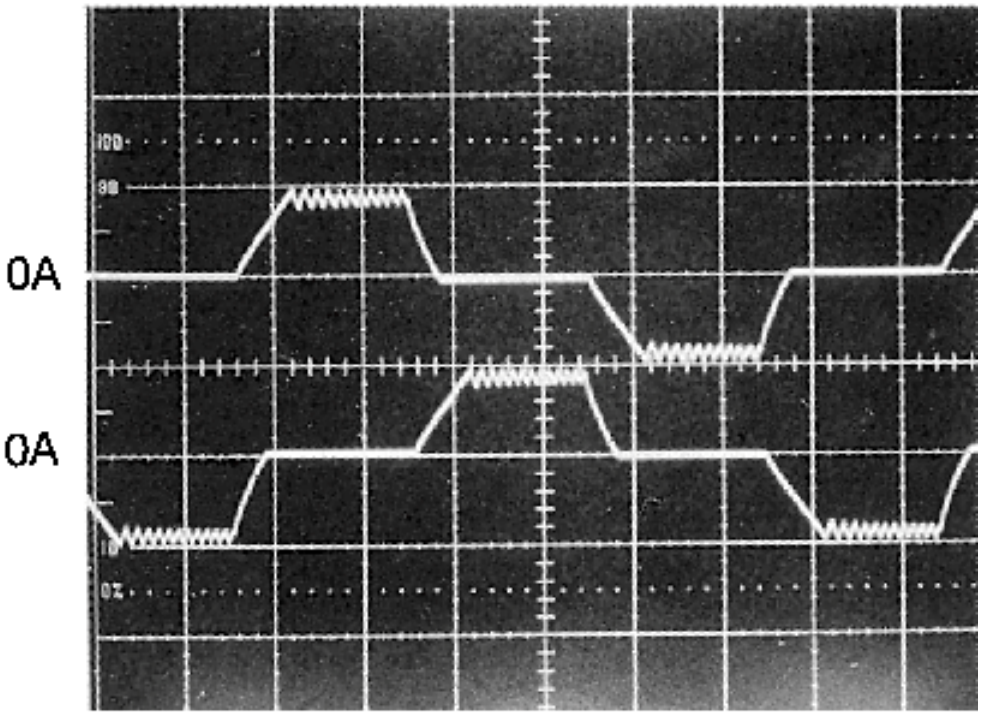
where A represents winding A energized with current in one direction and A* represents winding A energized with current in the opposite direction. The motor takes one full step each time one winding is de-energized and the other is energized. To make the motor step in the opposite direction, the order of the above sequence must be reversed. Figure 15 shows the winding currents and digital control signals for a wave drive application of the typical application circuit.

TWO-PHASE-ON FULL STEP DRIVE

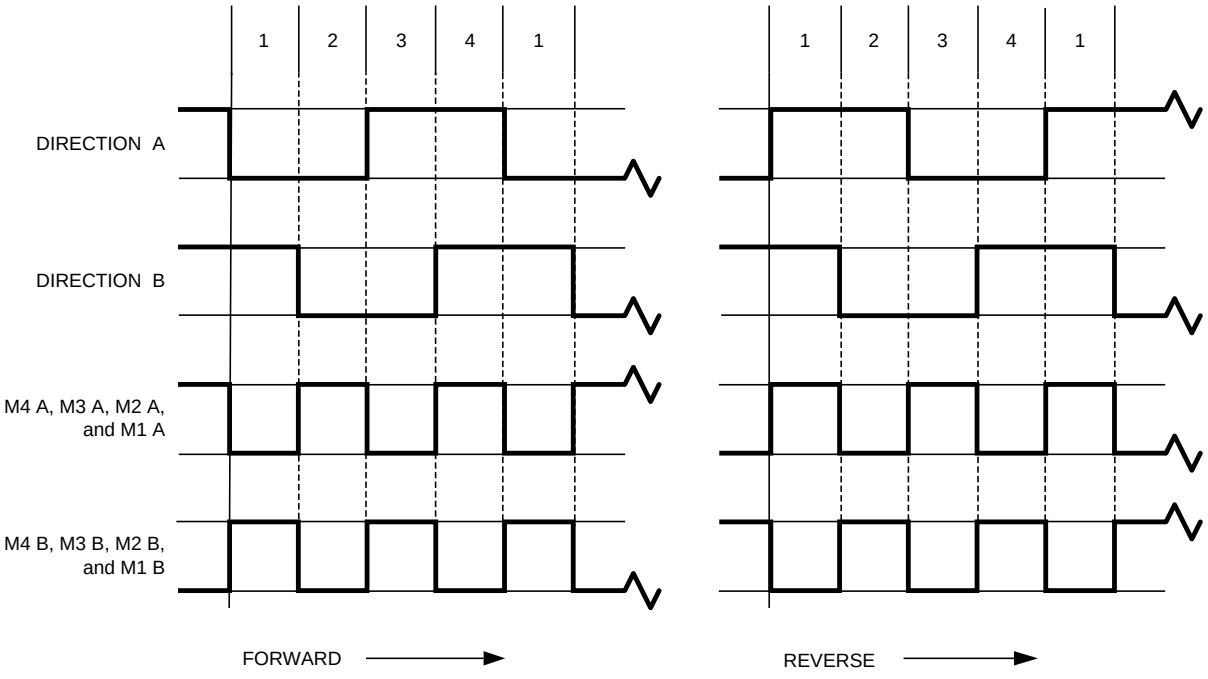
To make the motor take full steps, windings A and B can also be energized in the sequence

AB→A*B→A*B*→AB*→AB→ …,

and because both windings are energized at all times, this sequence produces more torque than that produced with wave drive. The motor takes one full step at each change of direction of either winding current. Figure 16 shows the winding currents and digital control signals for this application of the typical application circuit, and Figure 17 shows, for a single phase, the winding current and voltage at the output of the associated current sense amplifier.

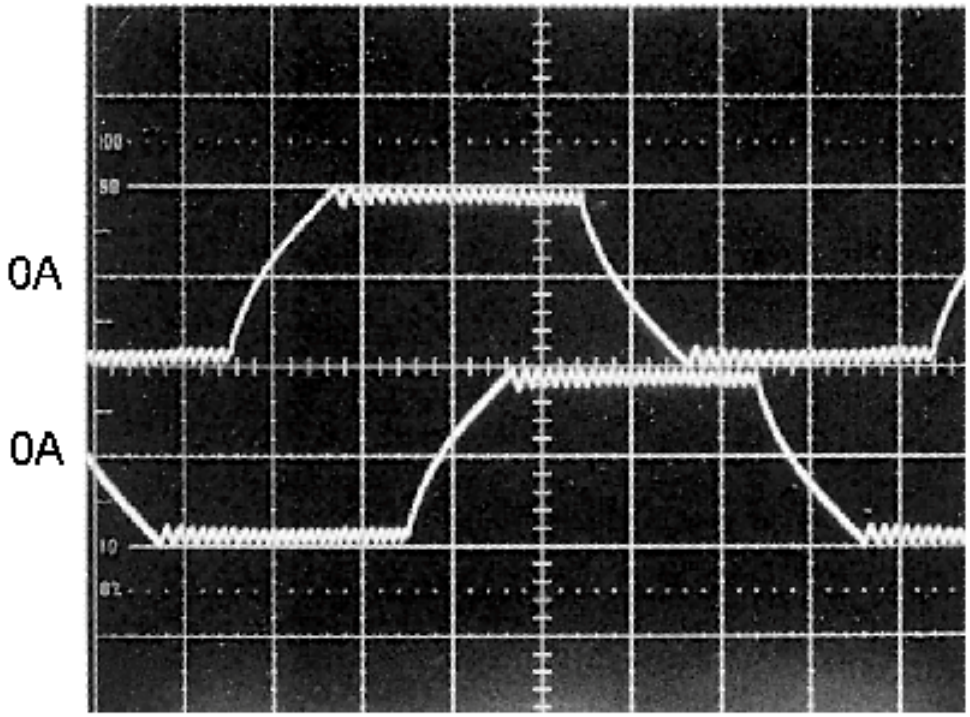


Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase B Winding Current at 1A/div
Horizontal: 1 ms/div
*500 steps/second

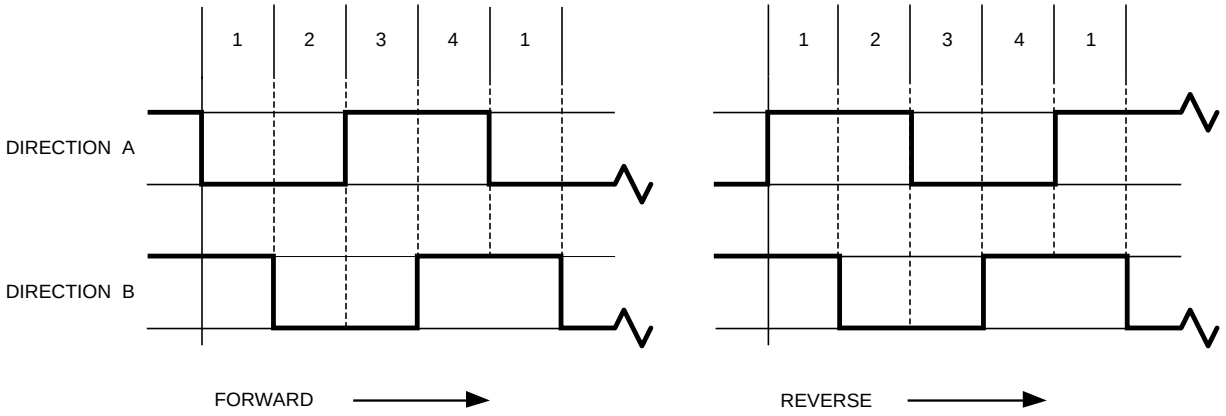


BRAKE A = BRAKE B = 0

Figure 15. Winding Currents and Digital Control Signals for One-Phase-On Drive (Wave Drive)

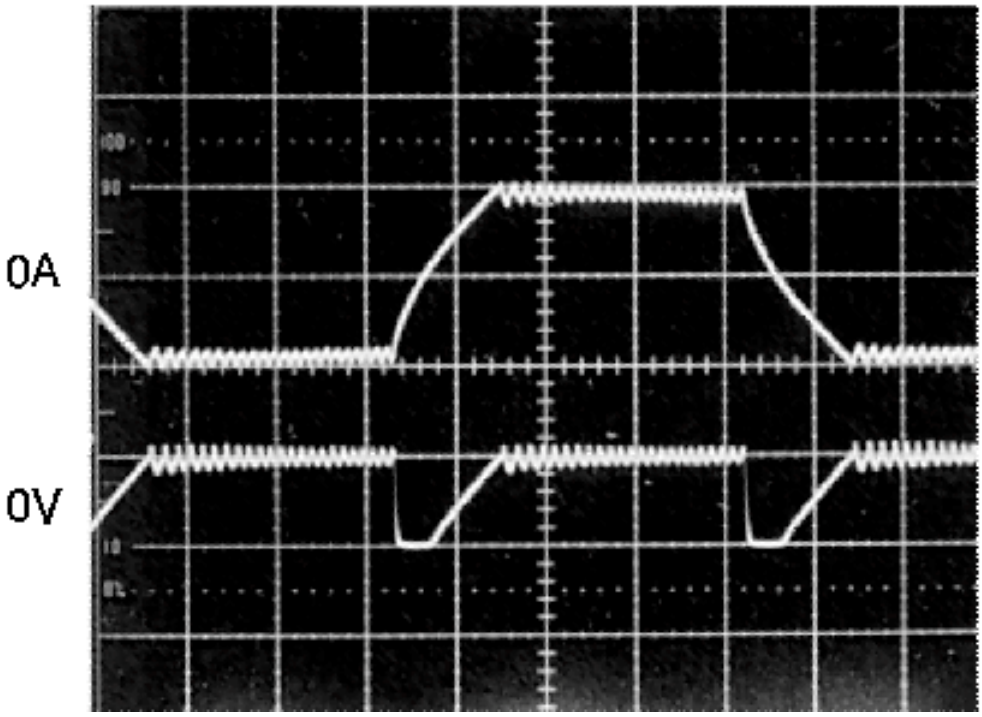


Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase B Winding Current at 1A/div
Horizontal: 1 ms/div
*500 steps/second



M4 A through M1 A = M4 B through M1 B = 1
BRAKE A = BRAKE B = 0

Figure 16. Winding Currents and Digital Control Signals for Two-Phase-On Drive



Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase A Sense Voltage at 5V/div
Horizontal: 1 ms/div
*500 steps/second

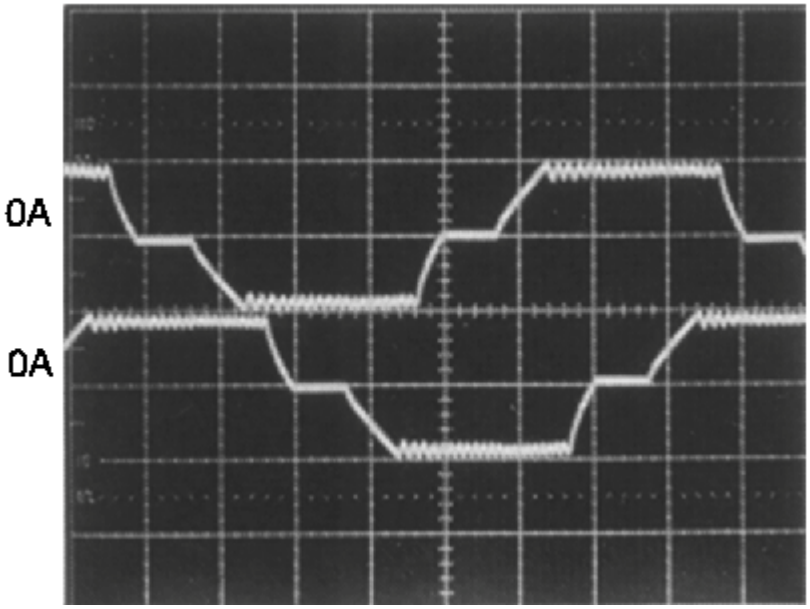
Figure 17. Winding Current and Voltage at the Output of the Associated Current Sense Amplifier

HALF STEP DRIVE WITHOUT TORQUE COMPENSATION

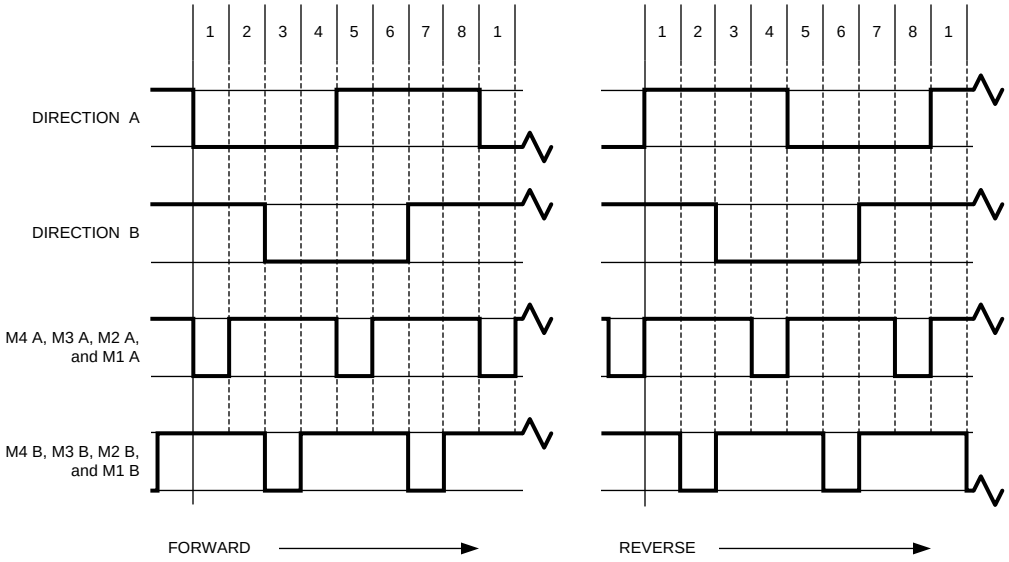
To make the motor take half steps, windings A and B can be energized in the sequence

A→AB→B→A*B→A*→
A*B*→B*→AB*→A→ …

The motor takes one half step each time the number of energized windings changes. It is important to note that although half stepping doubles the step resolution, changing the number of energized windings from two to one decreases (one to two increases) torque by about 40%, resulting in significant torque ripple and possibly noisy operation. Figure 18 shows the winding currents and digital control signals for this half step application of the typical application circuit.



Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase B Winding Current at 1A/div
Horizontal: 1 ms/div
*500 steps/second



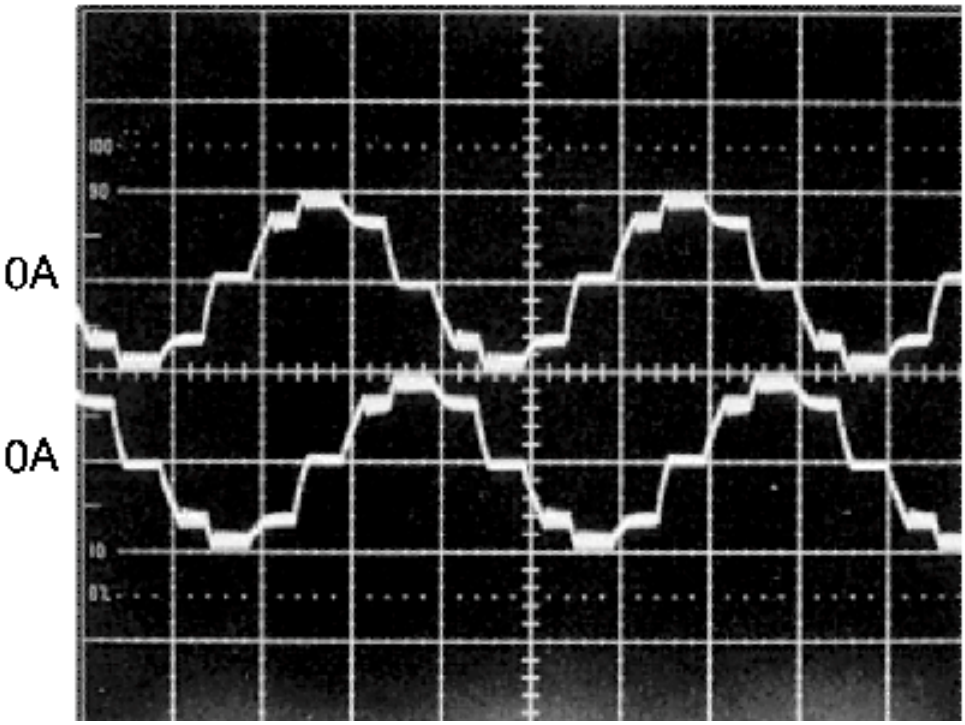
BRAKE A = BRAKE B = 0

Figure 18. Winding Currents and Digital Control Signals for Half Step Drive without Torque Compensation

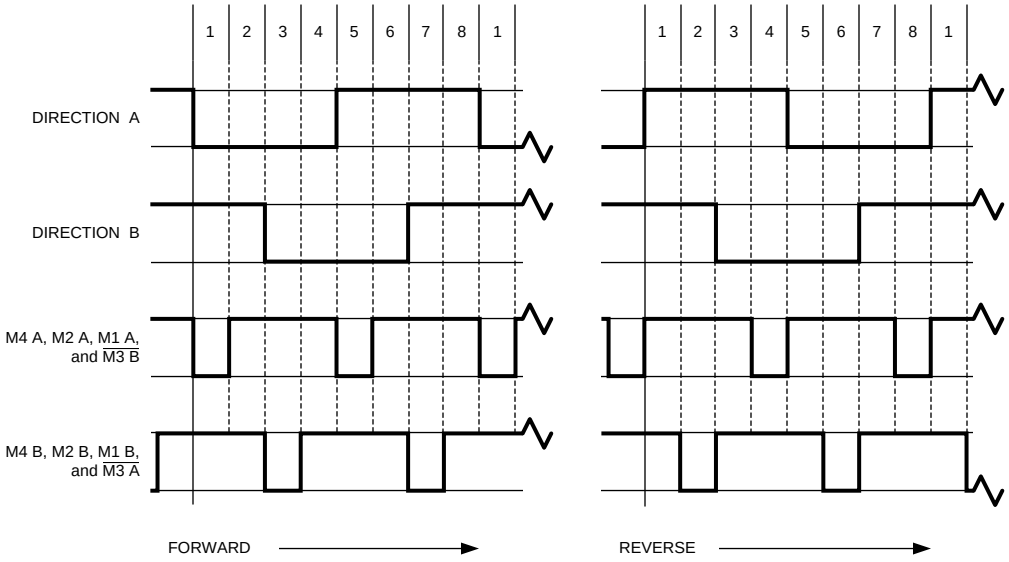
HALF STEP DRIVE WITH TORQUE COMPENSATION

To make the motor take half steps, the windings can also be energized with sinusoidal currents (Figure 19). Controlling the winding currents in the fashion shown doubles the step resolution without the significant torque ripple of the prior drive technique. The motor takes one half step each time the level of either winding current changes. Half step drive with torque compensation is microstepping drive. Along with the obvious advantage of increased step resolution, micro-stepping reduces both full step oscillations and resonances that occur as the motor and load combination is driven at its natural resonant frequency or subharmonics thereof. Both of these advantages are obtained by replacing full steps with bursts of microsteps. When compared to full step drive, the motor runs smoother and quieter.

Table 2 shows the lookup table for this application of the typical application circuit. Dividing 90°electrical per full step by two microsteps per full step yields 45° electrical per microstep. α, therefore, increases from 0 to 315° in increments of 45°. Each full 360° cycle comprises eight half steps. Rounding |cosα| to four bits gives D A, the decimal equivalent of the binary number applied at M4 A through M1 A. DIRECTION A controls the polarity of the current in winding A. Figure 19 shows the sinusoidal winding currents.



Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase B Winding Current at 1A/div
Horizontal: 2 ms/div
*500 steps/second



BRAKE A = BRAKE B = 0
90° ELECTRICAL/FULL STEP ÷ 2 MICROSTEPS/FULL STEP = 45° ELECTRICAL/MICROSTEP

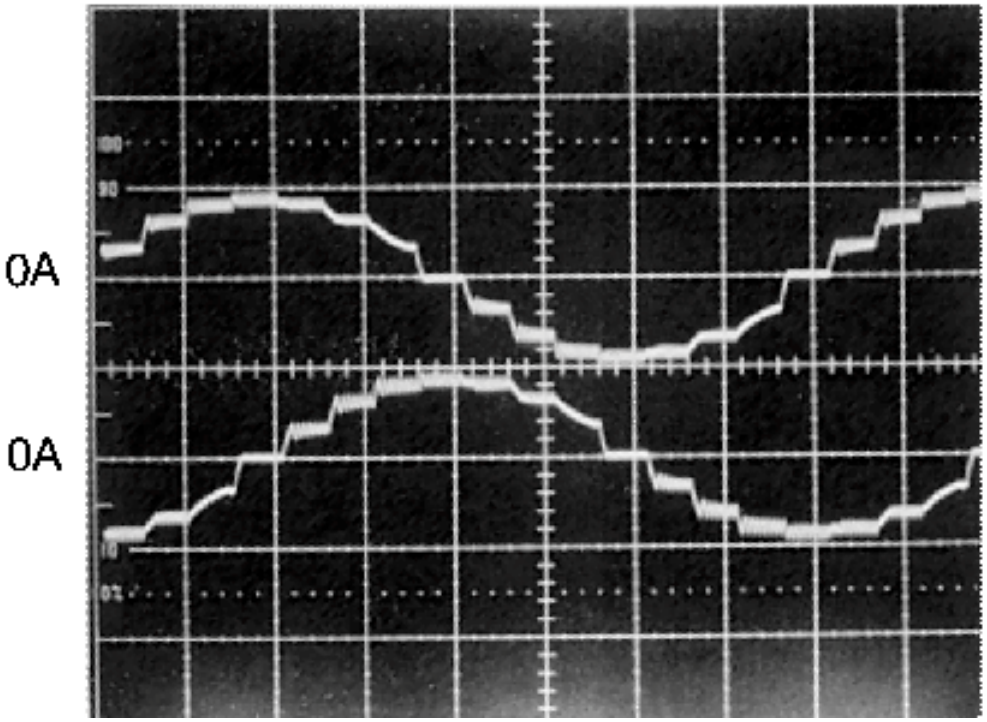
Figure 19. Winding Currents and Digital Control Signals for Half Step Drive with Torque Compensation

Table 2. Lookup Table for Half Step Drive with Torque Compensation

	α	|cos(α)|	D A	DIRECTION A	|sin(α)|	D B	DIRECTION B
|	0°	1	15	1	0	0	1
FORWARD	45°	0.707	11	1	0.707	11	1
↓	90°	0	0	0	1	15	1
	135°	0.707	11	0	0.707	11	1
	180°	1	15	0	0	0	0
↑	225°	0.707	11	0	0.707	11	0
REVERSE	270°	0	0	1	1	15	0
|	315°	0.707	11	1	0.707	11	0
	REPEAT						

QUARTER STEP DRIVE WITH TORQUE COMPENSATION

Figure 20 shows the winding currents and lookup table for a quarter step drive (four microsteps per full step) with torque compensation.



Top Trace: Phase A Winding Current at 1A/div
Bottom Trace: Phase B Winding Current at 1A/div
Horizontal: 2ms/div
*250 steps/second
90° ELECTRICAL/FULL STEP ÷ 4 MICROSTEPS/FULL STEP = 22.5° ELECTRICAL/MICROSTEP

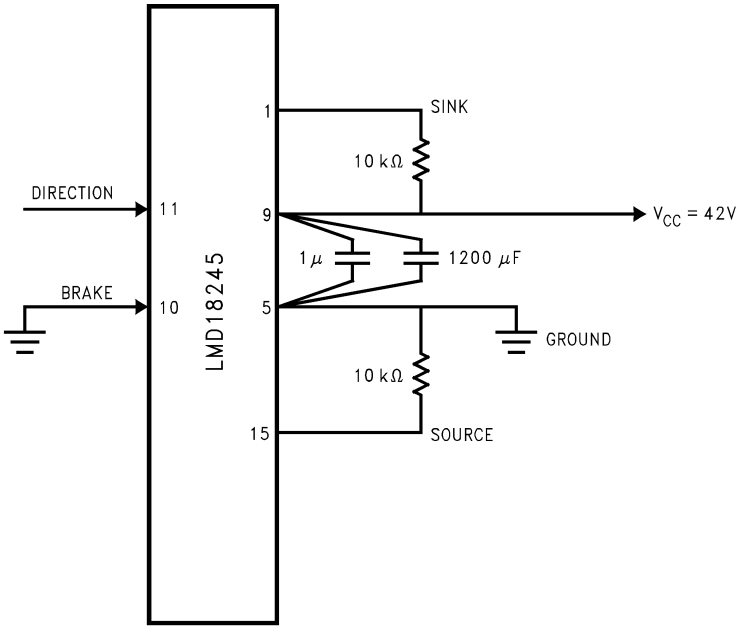
Figure 20. Winding Currents for Quarter Step Drive with Torque Compensation

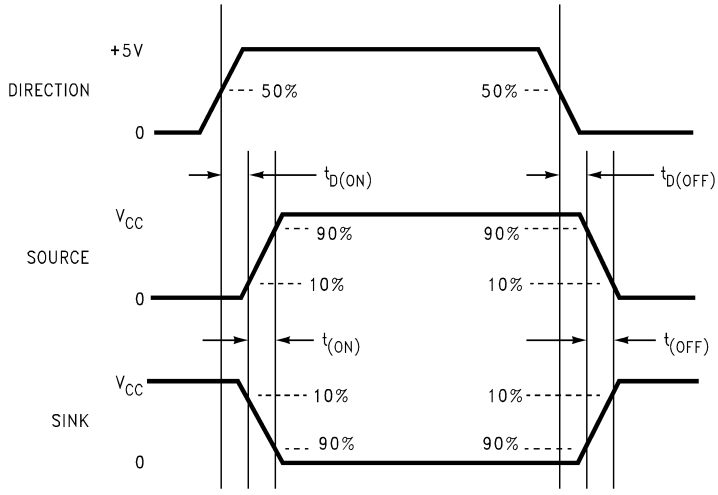
Table 3. Lookup Table for Quarter Step Drive with Torque Compensation(1)

	α	|cos(α)|	D A	DIRECTION A	|sin(α)|	D B	DIRECTION B
|	0.0°	1	15	1	0	0	1
FORWARD	22.5°	0.924	14	1	0.383	6	1
↓	45.0°	0.707	11	1	0.707	11	1
	67.5°	0.383	6	1	0.924	14	1
	90.0°	0	0	0	1	15	1
	112.5°	0.383	6	0	0.924	14	1
	135.0°	0.707	11	0	0.707	11	1
	157.5°	0.924	14	0	0.383	6	1
	180.0°	1	15	0	0	0	0
	202.5°	0.924	14	0	0.383	6	0
	225.0°	0.707	11	0	0.707	11	0
	247.5°	0.383	6	0	0.924	14	0
	270.0°	0	0	1	1	15	0
↑	292.5°	0.383	6	1	0.924	14	0
REVERSE	315.0°	0.707	11	1	0.707	11	0
|	337.5°	0.924	14	1	0.383	6	0
	REPEAT						

(1) BRAKE A = BRAKE B = 0

Test Circuit and Switching Time Definitions





REVISION HISTORY

Changes from Revision D (April 2013) to Revision E	Page
• Changed layout of National Data Sheet to TI format	25

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LMD18245T	NRND	TO-220	NDL	15	20	TBD	Call TI	Call TI	-40 to 125	LMD18245T P+	
LMD18245T/NOPB	ACTIVE	TO-220	NDL	15	20	Green (RoHS & no Sb/Br)	SN	Level-1-NA-UNLIM	-40 to 125	LMD18245T P+	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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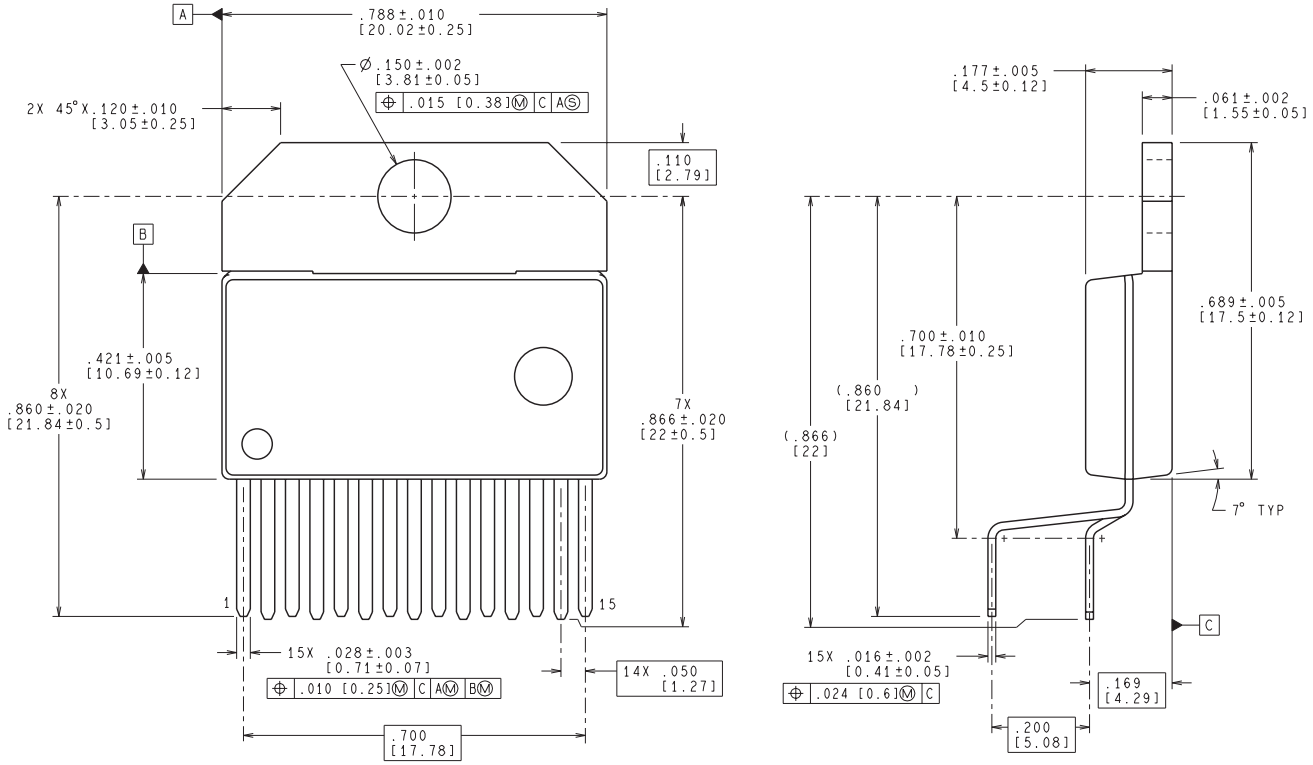

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